MC14502B

Strobed Hex Inverter/Buffer

The MC14502B is a strobed hex buffer/inverter with 3–state outputs, an inhibit control, and guaranteed TTL drive over the temperature range. The 3–state output simplifies design by allowing a common bus.

- Separate Output Disable Control
- 3–State Output
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 4LSTTL Loads Over the Rated Temperature Range

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648
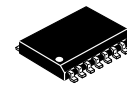
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

$T_A = -55°$ to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Pin	± 10	mA
I_{out}	Output Current (DC or Transient), per Pin	$+30$	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
    Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
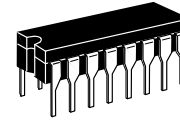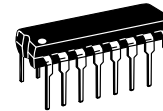   Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

LOGIC DIAGRAM

V_{DD} = PIN 16
V_{SS} = PIN 8

CIRCUIT DIAGRAM

Other five buffers are identical

TRUTH TABLE

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

MOTOROLA

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0"' Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current ($V_{OH} = 2.5$ Vdc) Source ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	− 3.0	—	− 2.4	− 4.2	—	− 1.7	—	mAdc
		5.0	− 0.64	—	− 0.51	− 0.88	—	− 0.36	—	
		10	− 1.6	—	− 1.3	− 2.25	—	− 0.9	—	
		15	− 4.2	—	− 3.4	− 8.8	—	− 2.4	—	
($V_{OL} = 0.4$ Vdc) Sink ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OL}	5.0	3.5	—	2.8	6.6	—	2.0	—	mAdc
		10	7.8	—	6.3	17	—	4.4	—	
		15	29	—	24	66	—	16	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance ($V_{in} = 0$)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (2.7\ \mu A/kHz)\ f + I_{DD}$							μAdc
		10	$I_T = (5.3\ \mu A/kHz)\ f + I_{DD}$							
		15	$I_T = (8.0\ \mu A/kHz)\ f + I_{DD}$							
Three–State Leakage Current	I_{TL}	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.006.

PIN ASSIGNMENT

D3	1 •	16 V_{DD}
Q3	2	15 D6
D1	3	14 Q6
DISABLE	4	13 D5
Q1	5	12 INH
D2	6	11 Q5
Q2	7	10 D4
V_{SS}	8	9 Q4

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

| Characteristic | Symbol | V_{DD} | All Types | | | Unit |
			Min	Typ #	Max	
Output Rise Time	t_{TLH}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Output Fall Time	t_{THL}	5.0 10 15	— — —	40 20 15	80 40 30	ns
Propagation Delay Time Data to Q	t_{PHL}	5.0 10 15	— — —	135 55 40	270 110 80	ns
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0 10 15	— — —	335 145 95	670 290 190	ns
Propagation Delay Time Data to Q, Inhibit to Q	t_{PLH}	5.0 10 15	— — —	295 130 95	590 260 190	ns
3–State Propagation Delay, Output "1" to High Impedance	t_{PHZ}	5.0 10 15	— — —	65 30 25	130 60 50	ns
3–State Propagation Delay, High Impedance to "1" Level	t_{PZH}	5.0 10 15	— — —	260 105 80	520 210 160	ns
3–State Propagation Delay, Output "0" to High Impedance	t_{PLZ}	5.0 10 15	— — —	150 70 55	300 140 110	ns
3–State Propagation Delay, High Impedance to "0" Level	t_{PZL}	5.0 10 15	— — —	160 65 50	320 130 100	ns

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
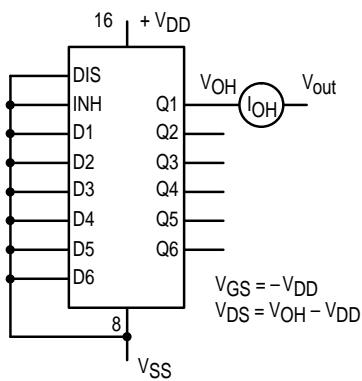

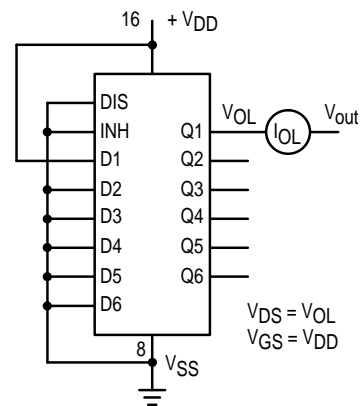**Figure 1. Typical Output Source
Current Test Circuit (I_{OH})**

$V_{GS} = -V_{DD}$
$V_{DS} = V_{OH} - V_{DD}$

**Figure 2. Typical Output Sink
Current Test Circuit (I_{OL})**

$V_{DS} = V_{OL}$
$V_{GS} = V_{DD}$
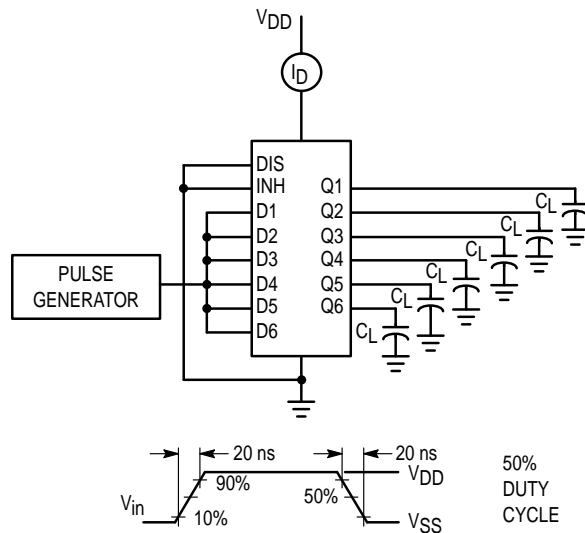
Figure 3. Power Dissipation Test Circuit and Waveform

Switch Positions for 3–State Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open
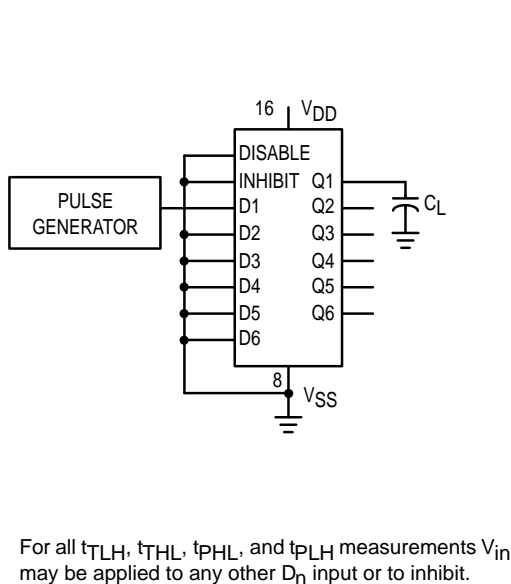
For all t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH} measurements V_{in} may be applied to any other D_n input or to inhibit.
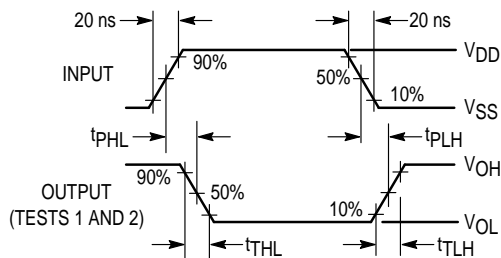
Figure 4. AC Test Circuit and Waveforms
(t_{TLH}, t_{THL}, T_{PLH}, and t_{PHL})
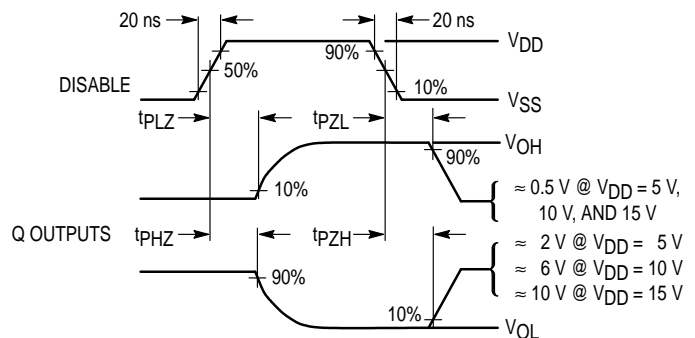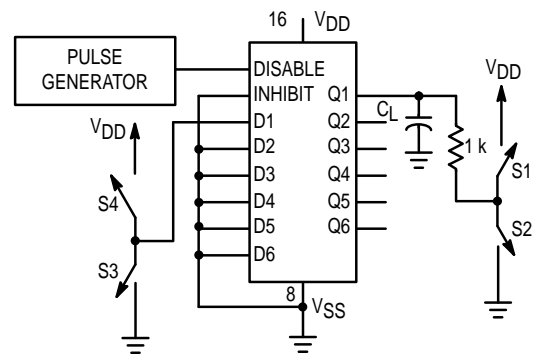
Figure 5. 3–State AC Test Circuit and Waveforms
(t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL})

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V
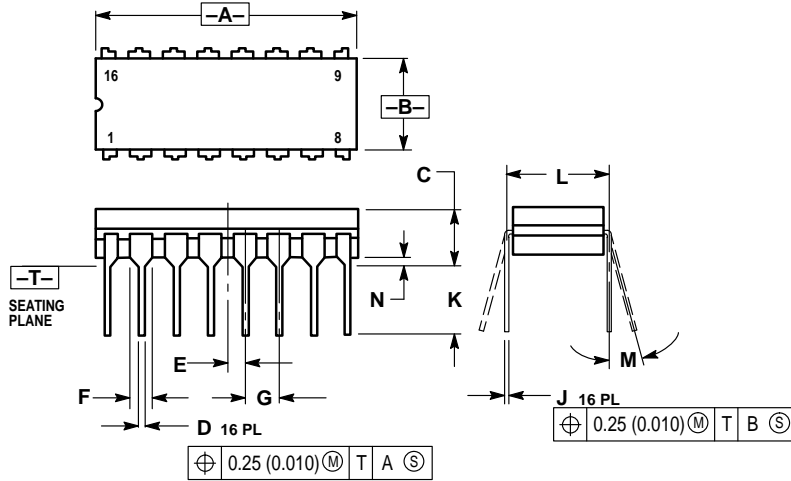
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R
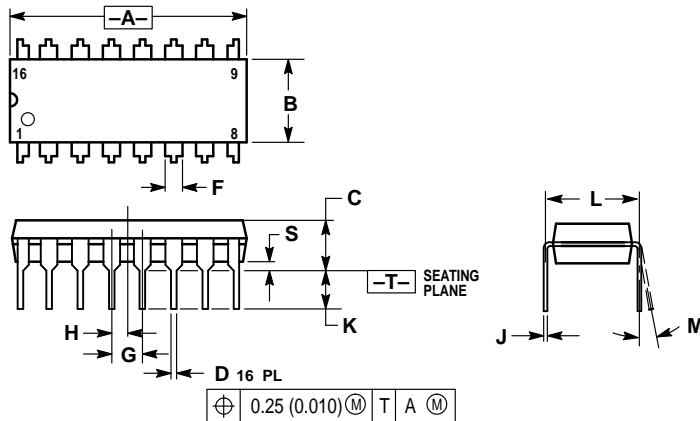
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A
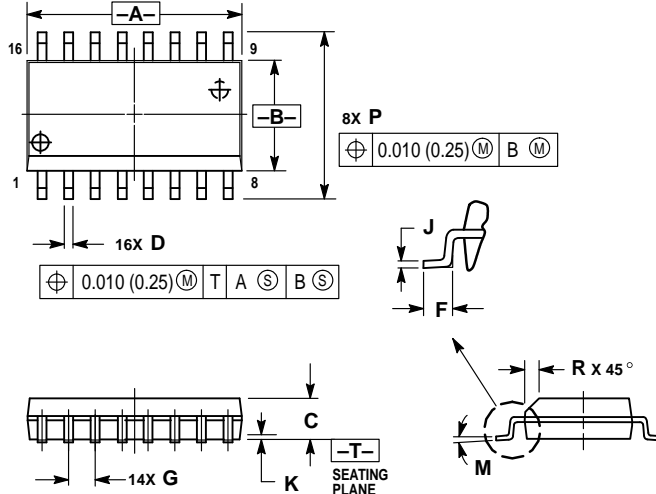
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

8X **P**

$\oplus$ | 0.010 (0.25) Ⓜ | B | Ⓜ

16X **D**

$\oplus$ | 0.010 (0.25) Ⓜ | T | A Ⓢ | B Ⓢ

14X **G**

SEATING PLANE

R x 45°

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Ⓜ **MOTOROLA**

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MC14502B/D