CMOS 4-BIT MICROCONTROLLER

TMP47C1237N, TMP47C1637N

The 47C1237/1637 are based on the TLCS-470A series. The 47C1237/1637 have on-screen display circuit (OSD) to display characters and marks which indicate channel or time on TV screen, A/D converter input, D/A converter output such as TV.

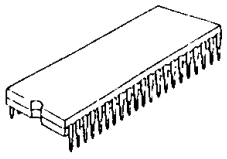
PART No.	ROM	RAM	PACKAGE	PIGGYBACK (adapter socket)
TMP47C1237N	12288 x 8-bit	512 x 4-bit	SDIP42	*TMP47C038E (BM1105)
TMP47C1637N	16384 x 8-bit			

* : Under Development

FEATURES

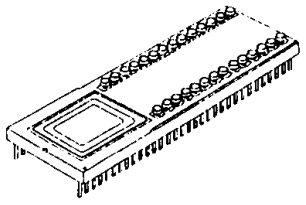
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.3μs (at 6MHz), 244μs (at 32.8KHz)
- ◆105 basic instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available
- ◆I/O port (32 pins)
  - Input 3 ports 7 pins
  - I/O 7 ports 25 pins
- ◆Two 12-bit Timer/Counters
- ◆Interval Timer
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
- ◆On-screen display circuit
  - Character patterns : 128 Characters
  - Characters displayed : 20 columns x 4 lines
  - Composition : 14 x 18 dots (80 Characters)
    7 x 9 dots (48 Characters)
  - Size of character : 3 kinds (line by line)
  - Color of character : 7 kinds (character by character)
  - Variable display position : Horizontal/Vertical 128 steps
  - Fringing, Smoothing function
- ◆D/A converter (Pulse width modulation) outputs
  - 14-bit resolution 1 channel
  - 7-bit resolution 7 channels
- ◆4-bit A/D converter input (4 Channels)
- ◆Horizontal synchronous signal is detected by timer/counter
- ◆Pulse output (Clock for PLL IC)
- ◆Remote control signal preprocessing capability
- ◆High current outputs : LED direct drive (typ. 20mA x 4 bits)
- ◆Dual-clock operation
  High-speed/low-power consumption operating mode
- ◆Hold function : Battery/Capacitor back-up
- ◆Real Time Emulator : BM47C1638

SDIP42



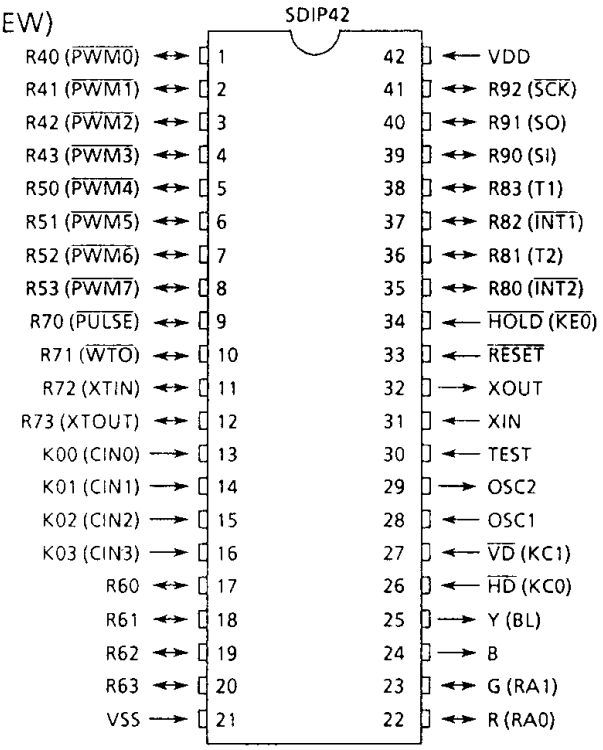
TMP47C1237N
TMP47C1637N

SDIC64

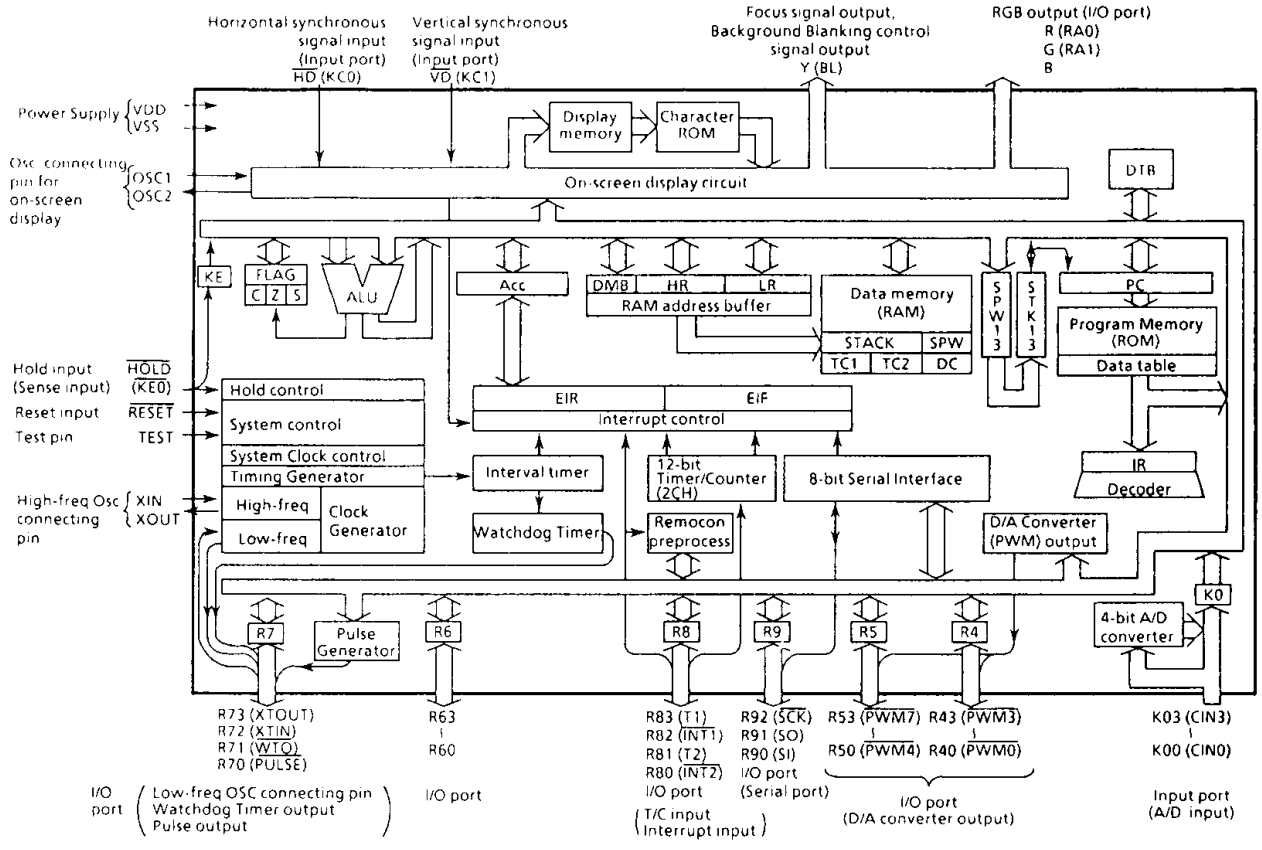


TMP47C038E

PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (CIN3) -K00 (CIN0)	Input (Input)	4-bit input port.	A/D conversion (Comparator) input
R43 ($\overline{PWM3}$) -R41 ($\overline{PWM1}$)	I/O (Output)	4-bit I/O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1".	7-bit D/A converter (PWM) output
R40 ($\overline{PWM0}$)			14-bit D/A converter (PWM) output
R53 ($\overline{PWM7}$) -R50 ($\overline{PWM4}$)	I/O (Output)		7-bit D/A converter (PWM) output
R63 - R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When used as input port watchdog output pin, or pulse output pin, the latch must be set to "1".	Resonator connecting pin (Low frequency)
R72 (XTIN)	I/O (Input)		
R71 ($\overline{WTO}$)	I/O (Output)		Watchdog timer output
R70 ($\overline{PULSE}$)			Pulse output (Clock for PLL IC)
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 or REMO-CON input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
G (RA1)	Output (I/O)	RGB output	2-bit I/O port with latch. When used as input port, the latch must be set to "1".
R (RA0)			
B	Output		
Y (BL)	Output	Focus signal output	Background blanking control signal output
$\overline{HD}$ (KC0)	Input	Horizontal synchronous signal input.	2-bit input port
$\overline{VD}$ (KC1)		Vertical synchronous signal input.	
OSC1, OSC2	Input, Output	Resonator connecting pin of on-screen display circuit.	
XIN, XOUT		Resonator connecting pin (High frequency). For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power Supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

The 47C1237/1637 are the same as the 47C1238/1638 except for the addition of RA port and the reduction of P1, P2, R3 and BL ports. And the Y/BL pin is used for both Y signal and BL signal output. The other functions and operation are exactly the same. Refer to the technical data sheets for the 47C1238/1638 and 47C1260/1660.

1. Input / Output Ports

The 47C1237 / 1637 have 10 built-in input/output ports (32 pins) as follows:

① K0	;	4-bit input	(also used for comparator input)
② R4, R5	;	4-bit input / output	(also used for pulse width modulation output)
③ R6	;	4-bit input / output	
④ R7	;	4-bit input / output	(also used for resonator connection, watchdog timer output, pulse output)
⑤ R8	;	4-bit input / output	(also used for external interrupt input, timer/counter input)
⑥ R9	;	3-bit input / output	(also used as a serial port)
⑦ RA	;	2-bit input / output	(shared by on-screen display output)
⑧ KC	;	2-bit input	(also used for horizontal and vertical sync. signal input)
⑨ KE	;	1-bit sense input	(also used for hold request / release signal input)

This section describes ports of ③ and ⑦ which are changed from 47C1238/1638.
Table 1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port R6 (R63-R60)

Ports R6 are 4-bit high current output ports which can directly drive LEDs, with 4-bit latches.

(2) Port RA (RA1, RA0)

R signal output and G signal output ports are also used as I/O ports. When not used for color signals, use is possible as normal I/O ports. RA port and Y/BL selection is performed by OP0A.
"1" is read out when the upper 2bits of IP0A are accessed.
As RA port is not selected, "1" is read out when the lower 2bits of IP0A are accessed.

Port address OP0A (Initial value 0011)

3	2	1	0
COSD		OP0A1	OP0A0

OP0A1/0	RA1/0 output

Port address IP0A

3	2	1	0
		IP0A1	IP0A0

IP0A1/0	RA1/0 input

COSD	control of OSD output and RA port

OP0A3	OP0A2	output pin No.			
		22	23	24	25
0	0	R	G	B	Y
0	1	RA0	G	B	B L
1	0	RA0	G	B	Y
1	1	RA0	RA1	B	B L

Figure 1. RA Port

2. D/A Converter (Pulse Width Modulation) Output

The 47C1237/1637 has 8 built-in pulse width modulation (PWM) channels. D/A converter output can easily be obtained by connecting an external low-pass filter.
$\overline{PWM}$ outputs are multiplexed with general purpose I/O ports as; R4 ($\overline{PWM0}$ - $\overline{PWM3}$), R5 ($\overline{PWM4}$ - $\overline{PWM7}$). When these ports are used as $\overline{PWM}$ outputs, the corresponding bits of R4 and R5 output latches should be set to "1". Resetting initializes the R4 and R5 output latches to "1".

Port Address (**)	Port		I/O instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	Tri-state (R4 port) Control	○	○	○	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note 3)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RA input port	RA output port	○	○	○	–	○	○	–
0B	——	——	–	–	–	–	–	–	–
0C	KC ($\overline{HD}$, $\overline{VD}$) input port	OSD command selector	○	○	○	–	–	○	–
0D	Remote control count value register	Remote control offset value register	○	○	○	–	–	–	–
0E	Status input (Note 2)	Remote control signal preprocess circuit control	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	$\overline{HOLD}$ Pin Status	Hold operation mode	○	○	–	–	–	–	–
11	——	——	–	–	–	–	–	–	–
12	——	A / D converter input control	–	○	–	–	–	–	–
13	SK0, DTB, Status	Tri-state, DTB, comparator	○	○	–	–	–	–	–
14	——	——	–	–	–	–	–	–	–
15	——	Watchdog timer control	–	○	–	–	–	–	–
16	——	System clock control	–	○	–	–	–	–	–
17	Status input for PWM	PWM buffer selector	○	○	–	–	–	–	–
18	——	PWM data transfer buffer	–	○	–	–	–	–	–
19	——	Interval timer interrupt control	–	○	–	–	–	–	–
1A	Display line counter	OSD control	○	○	–	–	–	–	–
1B	——	Pulse output control	–	○	–	–	–	–	–
1C	——	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	——	Timer/Counter 2 control	–	○	–	–	–	–	–
1E	——	SIO control 1	–	○	–	–	–	–	–
1F	——	SIO control 2	–	○	–	–	–	–	–

Note 1 . "——" means the reserved state. Unavailable for the user programs.

Note 2 . The status input of serial interface, clock generator, and $\overline{HOLD}$ ($\overline{KE0}$) pin.

Note 3 . The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 1. Port Address Assignments and Available I/O Instructions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include port R7	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports R6	30	mA
	I_{OUT2}	Ports R7, R8, R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports R6	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	f_{OSD}	OSC1, OSC2		−	8.0	

Note . Input Voltage V_{IH3}, V_{IL3}: in the HOLD operating mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Tri-state port Ports R6, R8, R9 (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	± 2	μA
Output High Voltage	V_{OH2}	Port R (tri-state), OSD outputs	V_{DD} = 4.5V, I_{OH} = − 0.7mA	4.1	−	−	V
Output Low Voltage	V_{OL1}	Ports R7, R8, R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	V
	V_{OL2}	Port R (tri-state), OSD outputs	V_{DD} = 4.5V, I_{OL} = 0.7mA				
Output Low Current	I_{OL}	Port R6	V_{DD} = 4.5V, V_{OL} = 1.0V	−	20	−	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, f_C = 4MHz	−	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained

Note 3. Supply Current : V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the pull − up / pull − down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog input voltage	V_{AIN}	CIN		V_{SS}	-	V_{DD}	V
A / D conversion error	-			-	-	$\pm\frac{1}{2}$	LSB

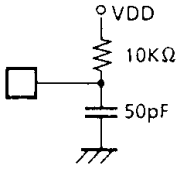
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

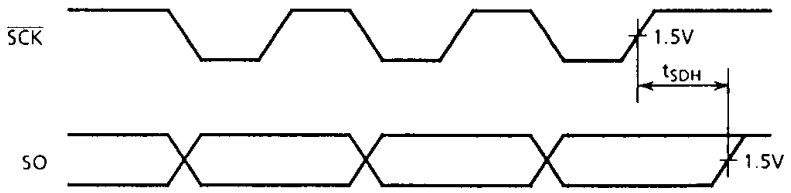
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.3	–	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		0.5tcy – 300	–	–	ns

Note. Shift data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin.



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

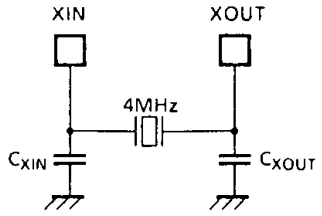
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 30 to 70°C)

(1) 4MHz
Ceramic Resonator

CSA4.00MG	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30pF

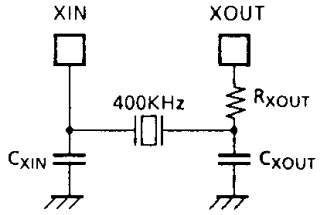
Crystal Oscillator

204B-8R 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20pF

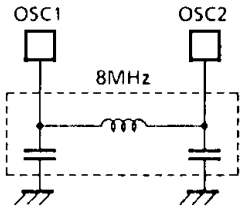


(2) 400KHz
Ceramic Resonator

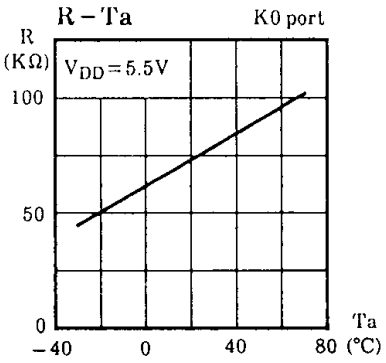
CSB400B	(MURATA)	$C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

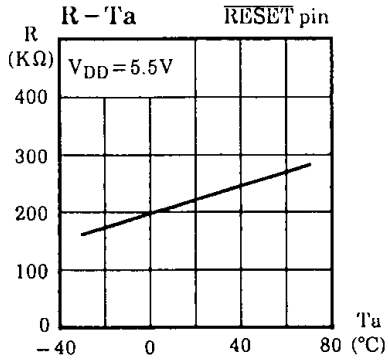


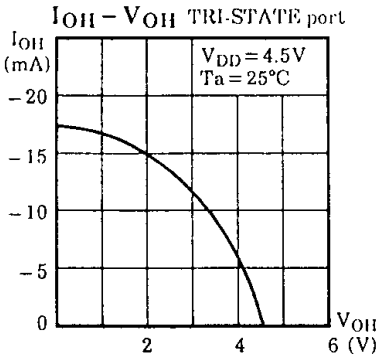
(3) 8MHz (for OSD)
LC Resonator

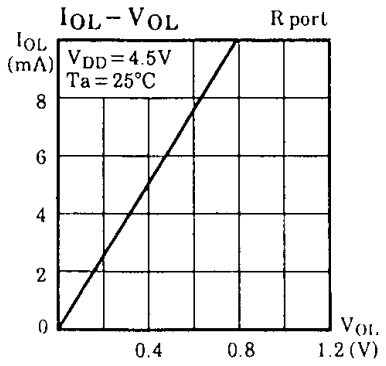


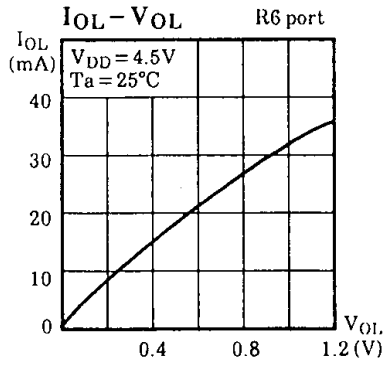
TYPICAL CHARACTERISTICS

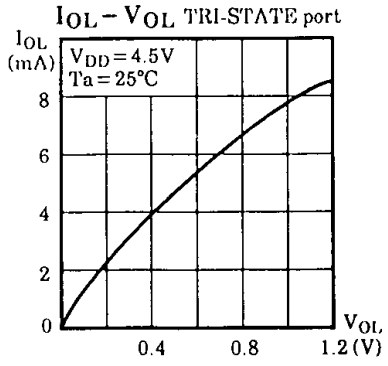


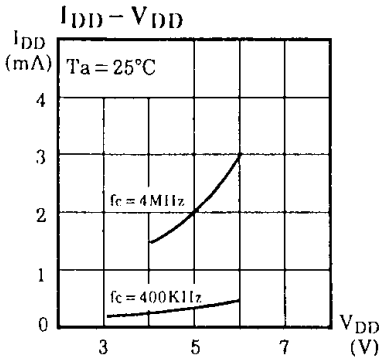


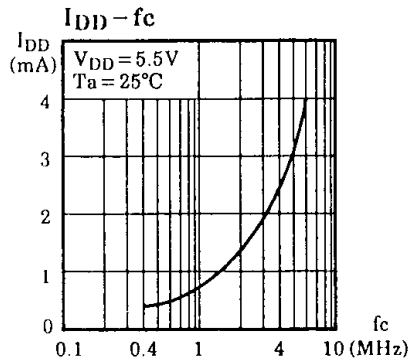












INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input/output circuitries of the 47C1237/1637 control pins are similar to that of the 47C1238/1638.

(2) I/O ports

The input/output circuitries of the 47C1237/1637 I/O ports are shown below, designated by code.

PORT	I/O	INPUT/OUTPUT CIRCUITRY (code)	REMARKS
K0	Input	PA: R PC: R, R_{IN}	Pull-down resistor R_{IN} = 70KΩ (typ.) R = 1KΩ (typ.)
R4 R5 RA	I/O	VDD, DISABLE, R	Tri-state I/O Initial "Hi-Z" R = 1KΩ (typ.)
R6	I/O	R	Sink open drain Initial "Hi-Z" High drive carrent I_{OL} = 20mA (typ.) R = 1KΩ (typ.)
R7 R8 R9	I/O	R7, R8, R9, R	Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) R = 1KΩ (typ.)
R (RA0) G (RA1)	I/O	VDD, DISABLE, R	Tri-state I/O Initial "Hi-Z" R = 1KΩ (typ.)
B Y (BL)	Output	VDD, DISABLE	Tri-state Output Initial "Hi-Z"