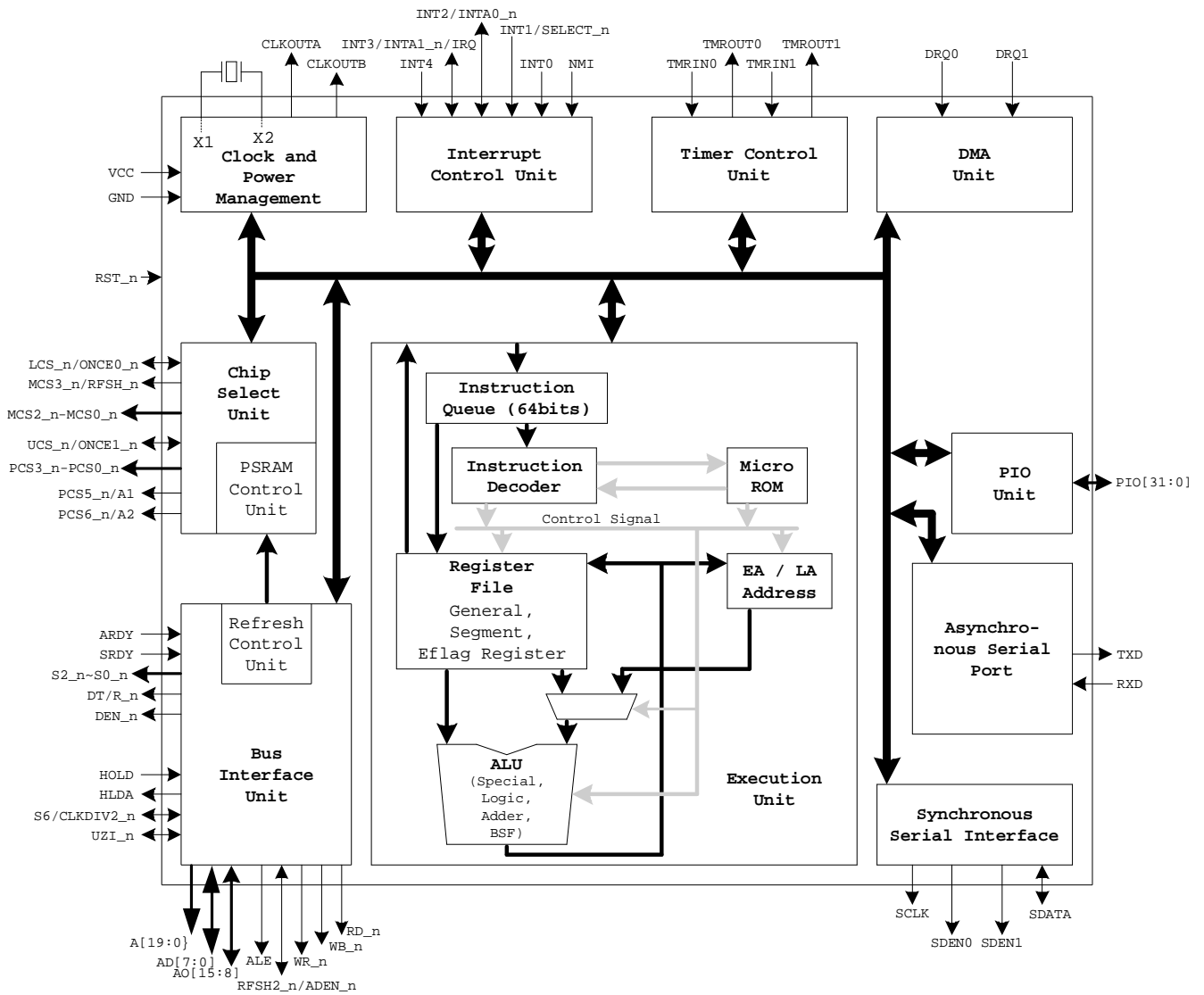


R8810
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

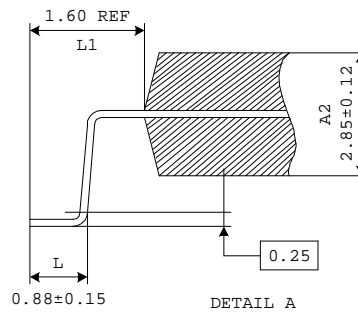
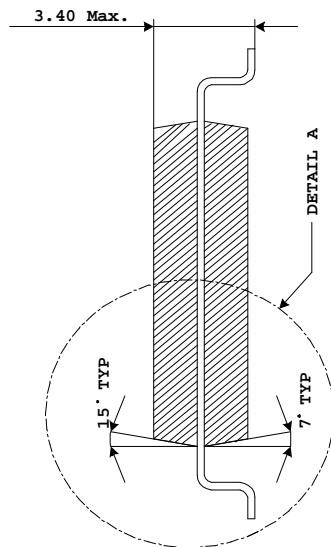
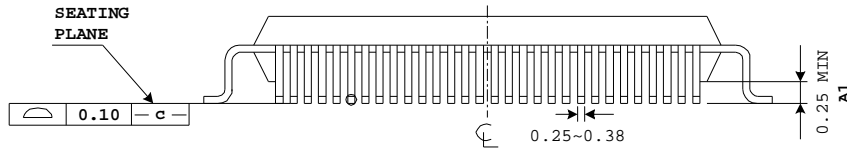
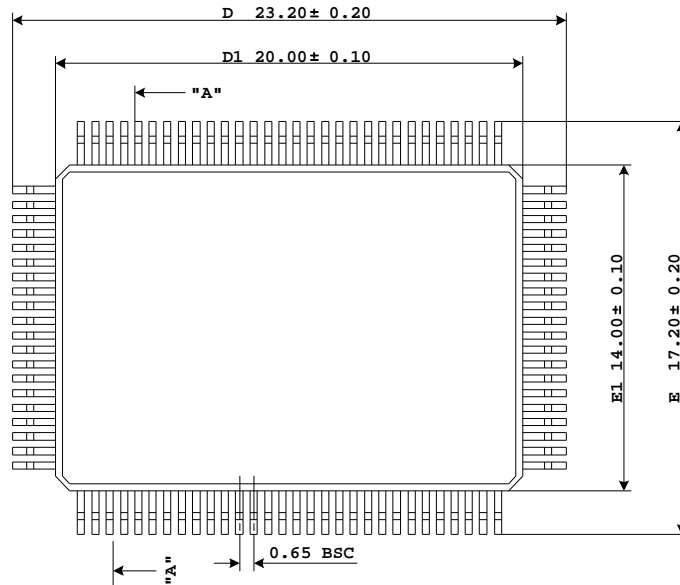
- I CPU Core**
 - RDC's proprietary RISC architecture
 - Five-stage pipeline
 - CPU clock speed up to 40 MHz
 - Supports CPU ID
 - Supports 32 PIO pins
 - Static & synthesizable design
- I Bus Interface**
 - A multiplexed address and data bus which is compatible with the 80C188 microprocessor
 - Supports a non-multiplexed address bus A[19:0]
- I ROM/RAM Controller and Addressing Space**
 - 1M-byte memory address space
 - 64K-byte I/O space
- I PSRAM Interface**
 - PSRAM (Pseudo static RAM) interface with auto-refresh control
- I Two Independent DMA Channels**
- I Asynchronous Serial Channel**
 - Supports one asynchronous serial channel with one synchronous serial channel
- I Interrupt Controller**
 - The Interrupt controller with five maskable external interrupts and one non-maskable external interrupt
- I Programmable Chip-select Logic**
 - Programmable chip-select logic for memory or I/O bus cycle decoder
- I Programmable Wait-state Generator**
- I Counter/Timers**
 - Three independent 16-bit timers and Timer 1 can be programmed as a watchdog timer
- I Software is compatible with the 80C188 microprocessor**
- I Operating Voltage Range**
 - Core voltage: 5V ± 5%
 - I/O voltage: 5V ± 10%
- I Ambient Temperature: 0 ~ +70°C**
- I Package Type**
 - 100-pin PQFP
 - 100-pin LQFP
- I A Green Product**

2. Block Diagram



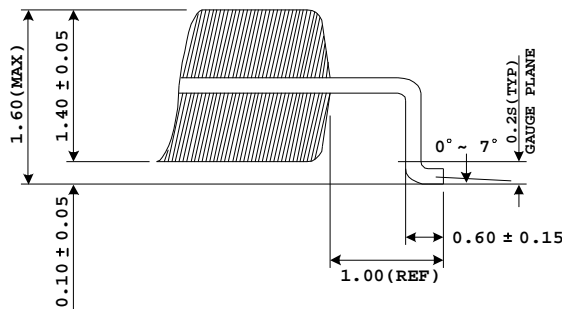
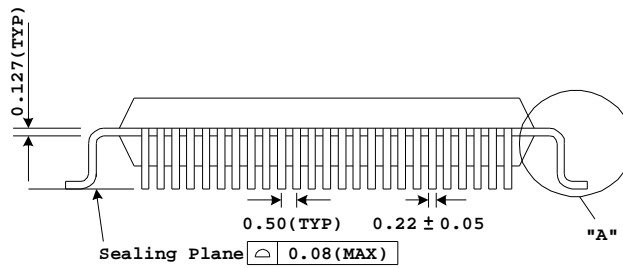
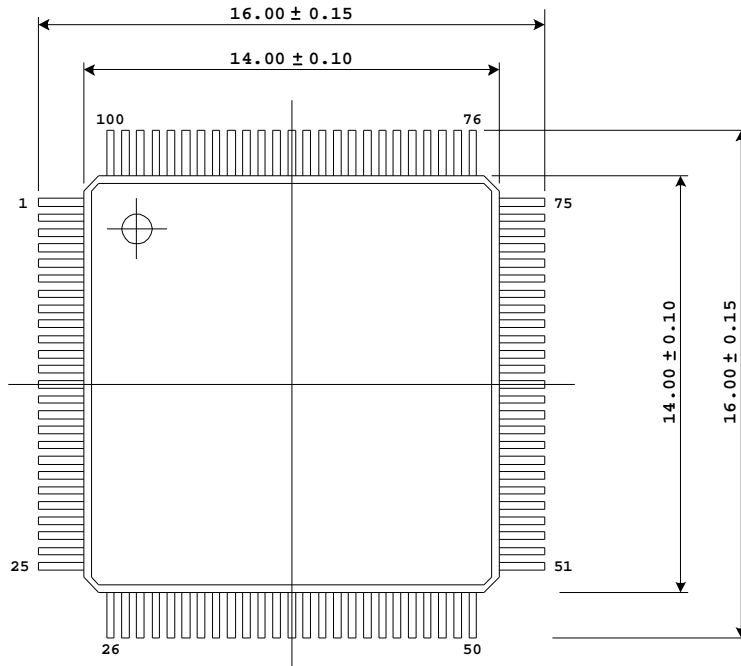
3. Package Information

PQFP 100 pins



UNIT : mm

LQFP 100 pins



UNIT : mm