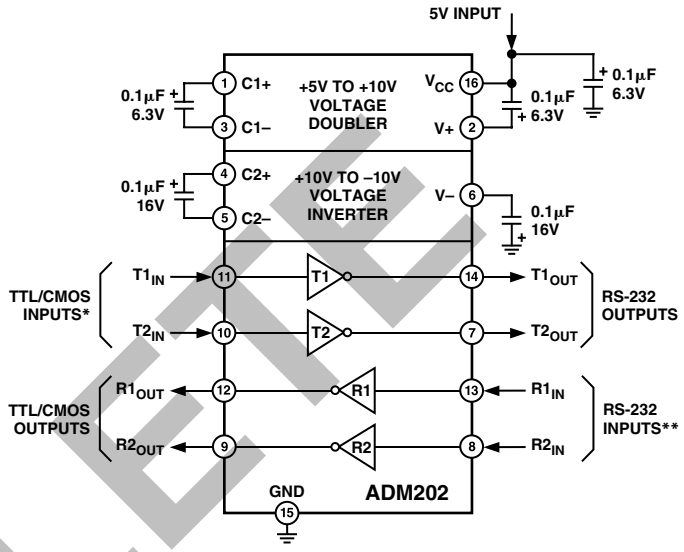
High-Speed, 5 V, 0.1 μF CMOS RS-232 Driver/Receivers

ADM203

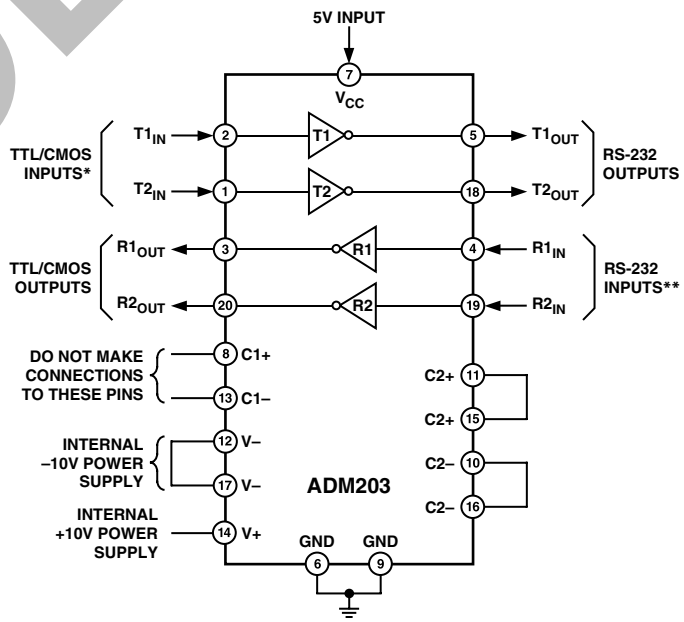
FEATURES
120 kB Transmission Rate
ADM202: Small (0.1 μF) Charge Pump Capacitors
ADM203: No External Capacitors Required
Single 5 V Power Supply
Meets EIA-232-E and V.28 Specifications
Two Drivers and Two Receivers
On-Board DC-DC Converters
±9 V Output Swing with 5 V Supply
Low Power BiCMOS: 2.0 mA I_{CC}
±30 V Receiver Input Levels

APPLICATIONS
Computers
Peripherals
Modems
Printers
Instruments

FUNCTIONAL BLOCK DIAGRAMS



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT.
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT.

GENERAL DESCRIPTION

The ADM202/ADM203 is a two-channel RS-232 line driver/receiver pair designed to operate from a single 5 V power supply. A highly efficient on-chip charge pump design permits RS-232 levels to be developed using charge pump capacitors as small as 0.1 μF. The capacitors are internal to the package on the ADM203 so no external capacitors are required. These converters generate ±10 V RS-232 output levels.

The ADM202/ADM203 meets or exceeds the EIA-232-E and V.28 specifications. Fast driver slew rates permit operation up to 120 kB while high-drive currents allow for extended cable lengths.

An epitaxial BiCMOS construction minimizes power consumption to 10 mW and also guards against latch-up. Overvoltage protection is provided allowing the receiver inputs to withstand continuous voltages in excess of ±30 V. In addition, all pins contain ESD protection to levels greater than 2 kV.

The ADM202 is available in 16-lead DIP and both narrow and wide SOIC packages. The ADM203 is available in a 20-lead DIP package.

REV. A

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ADM202/ADM203–SPECIFICATIONS (V_{CC} = 5 V ± 10%, (ADM202 C1–C4 = 0.1 µF). All Specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 5%, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
Output Voltage Swing	±5	±9		V	V_{CC} = 5 V ± 10%, T_A = 25°C, $T1_{OUT}$, $T2_{OUT}$ Loaded with 3 kΩ to GND
V_{CC} Power Supply Current		2.5	6.0	mA	No Load, $T1_{IN}$, $T2_{IN}$ = V_{CC} or $T1_{IN}$, $T2_{IN}$ = GND
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}
Input Logic Threshold High, V_{INH}	2.4			V	T_{IN}
Logic Pull-Up Current		12	25	µA	T_{IN} = 0 V
RS-232 Input Voltage Range	–30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	
RS-232 Input Threshold High		1.6	2.4	V	
RS-232 Input Hysteresis	0.2	0.4	1.0	V	
RS-232 Input Resistance	3	5	7	kΩ	T_A = 0°C to 85°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 1.6 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = –1.0 mA
Propagation Delay		0.3	5	µs	RS-232 to TTL
Transition Region Slew Rate		8		V/µs	R_L = 3 kΩ, C_L= 1000 pF Measured from +3 V to –3 V or –3 V to +3 V
Baud Rate	120			kB	R_L = 3 kΩ, C_L = 1 nF
Output Resistance	300			Ω	V_{CC} = V+ = V– = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10	±60	mA	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C unless otherwise noted)

V_{CC} . . . . . 6 V
V+ . . . . . (V_{CC} – 0.3 V) to +14 V
V– . . . . . +0.3 V to –14 V
Input Voltages
  T_{IN} . . . . . –0.3 V to (V_{CC} + 0.3 V)
  R_{IN} . . . . . ±30 V
Output Voltages
  T_{OUT} . . . . . (V+, +0.3 V) to (V–, – 0.3 V)
  R_{OUT} . . . . . –0.3 V to (V_{CC} + 0.3 V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
Power Dissipation
  N-16 DIP . . . . . 470 mW
  R-16N SOIC . . . . . 600 mW
  R-16W SOIC . . . . . 500 mW
  N-20 DIP . . . . . 890 mW
Thermal Impedance
  N-16 DIP . . . . . 135°C/W
  R-16N SOIC . . . . . 105°C/W
  R-16W SOIC . . . . . 105°C/W
  N-20 DIP . . . . . 125°C/W
Operating Temperature Range
  Commercial (J Version) . . . . . 0°C to 70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Soldering
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C
ESD Rating . . . . . >2000 V

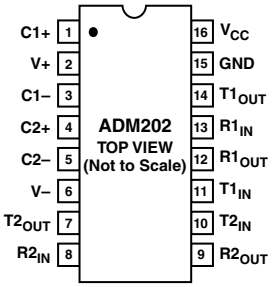
*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

ORDERING GUIDE

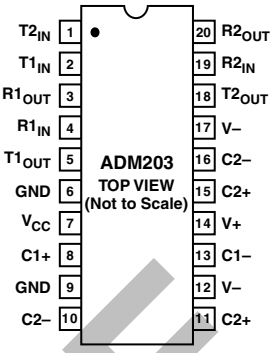
Model	Temperature Range	Package Option
ADM202JN	0°C to 70°C	N-16
ADM202JRN	0°C to 70°C	R-16N
ADM202JRW	0°C to 70°C	R-16W
ADM203JN	0°C to 70°C	N-20

PIN CONFIGURATIONS

DIP/SOIC



DIP



PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10%.
V+	Internally Generated Positive Supply (+10 V nominal).
V–	Internally Generated Negative Supply (–10 V nominal).
GND	Ground Pin. Must be connected to 0 V.
C1+	ADM202 External Capacitor, (+ terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C1–	ADM202 External Capacitor, (– terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C2+	ADM202 External Capacitor, (+ terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
C2–	ADM202 External Capacitor, (– terminal) is connected to this pin. ADM203: The capacitor is connected internally and no external capacitor is required.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each of these inputs.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.

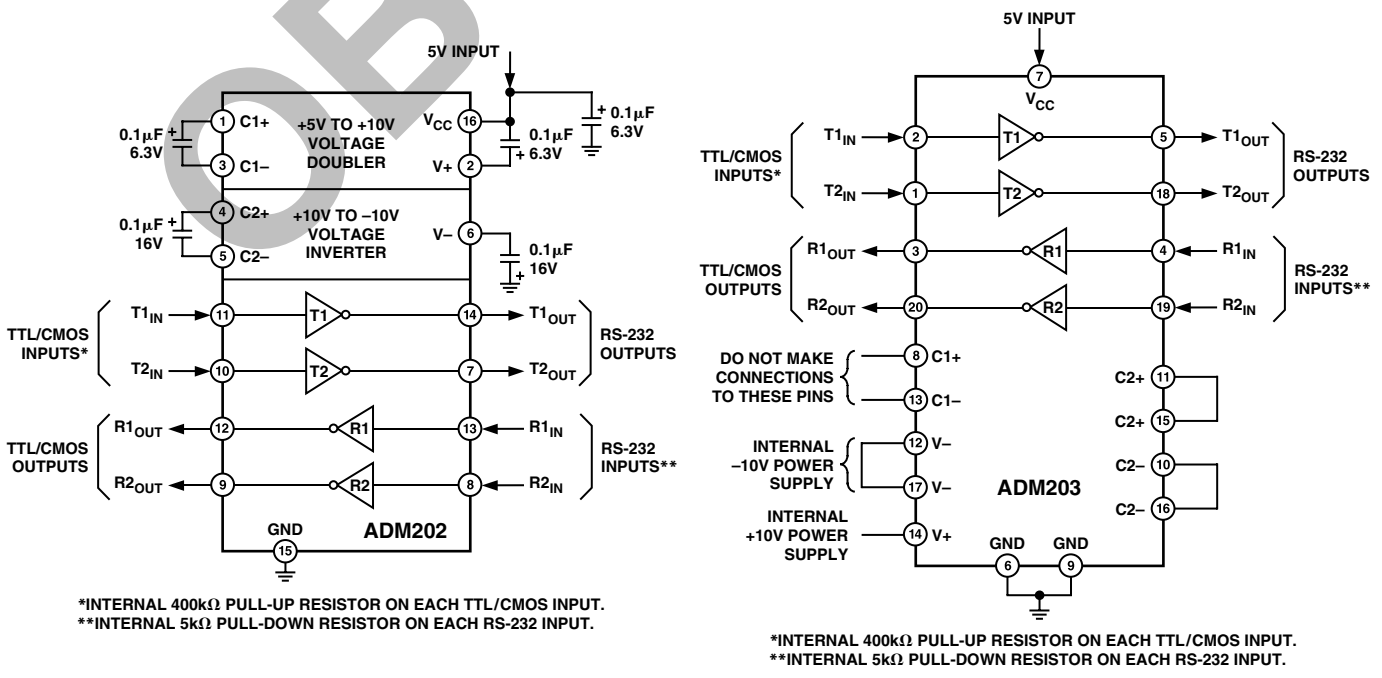
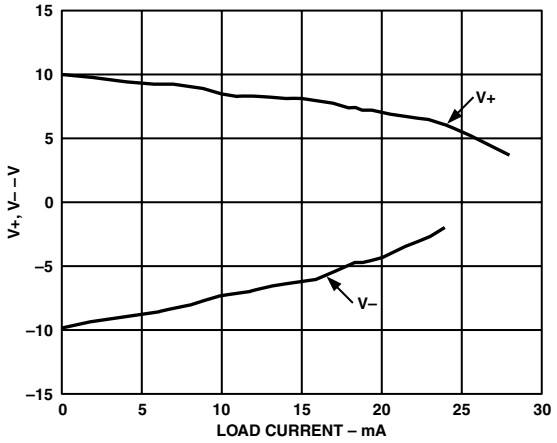
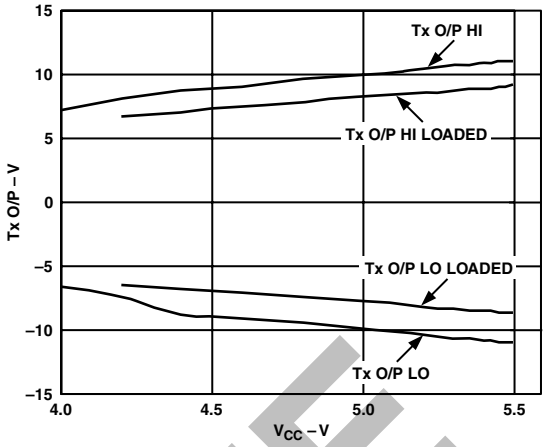


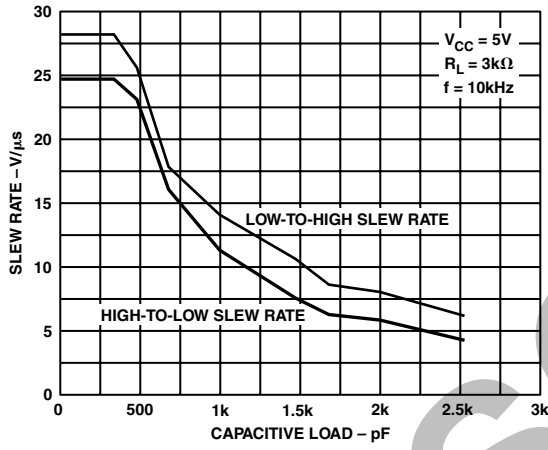
Figure 1. Typical Operating Circuits



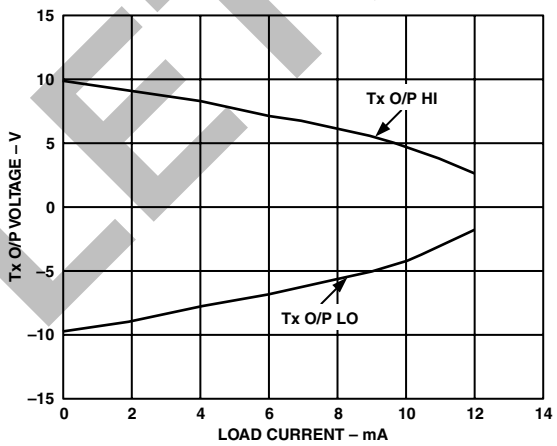
TPC 1. Charge Pump V+, V– vs. Current



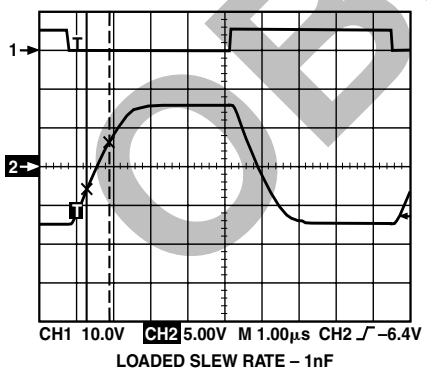
TPC 4. Transmitter Output Voltage vs. V_{CC}



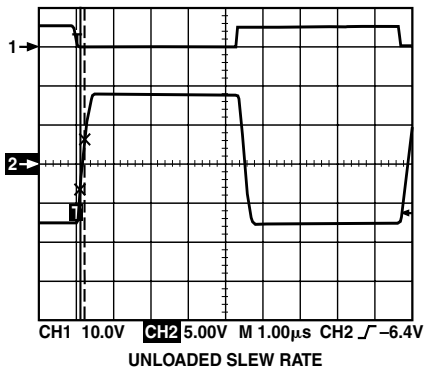
TPC 2. Transmitter Slew Rate vs. Load Capacitance



TPC 5. Transmitter Output Voltage vs. Current



TPC 3. Transmitter Fully Loaded Slew Rate



TPC 6. Transmitter Unloaded Slew Rate

GENERAL INFORMATION

The ADM202/ADM203 is an RS-232 drivers/receivers designed to solve interface problems by meeting the EIA-232E specifications while using a single digital 5 V supply. The EIA standard requires transmitters that will deliver ±5 V minimum on the transmission channel and receivers that can accept signal levels down to ±3 V. The parts achieve this by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum.

The ADM203 uses internal capacitors and, therefore, no external capacitors are required.

The ADM202 contains an internal voltage doubler and a voltage inverter which generates ±10 V from the 5 V input. External 0.1 µF capacitors are required for the internal voltage converter.

The ADM202/ADM203 is a modification, enhancement and improvement to the AD230–AD241 family and derivatives thereof. It is essentially plug-in compatible and does not have materially different applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of three main sections. These are:

(a) A Charge Pump Voltage Converter

(b) RS-232 to TTL/CMOS Receivers

(c) TTL/CMOS to RS-232 Transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated below. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate –10 V using C2 as the storage element.

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V– supplies. On the ADM203, all capacitors C1 to C4 are molded into the package.

The V+ and V– supplies may also be used to power external circuitry if the current requirements are small.

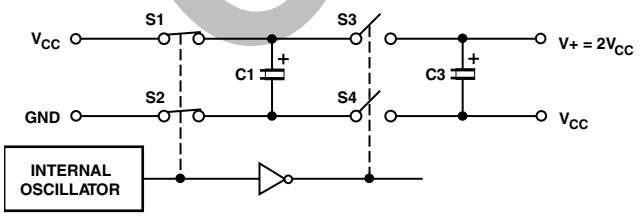


Figure 2. Charge Pump Voltage Doubler

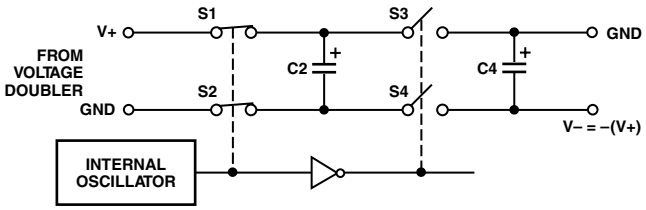


Figure 3. Charge Pump Voltage Inverter

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into EIA-232-E output levels. With V_{CC} = +5 V and driving a typical EIA-232-E load, the output voltage swing is ±9 V. Even under worst-case conditions the drivers are guaranteed to meet the ±5 V EIA-232-E minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the EIA-232-E standard the slew rate is limited to less than 30 V/µs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

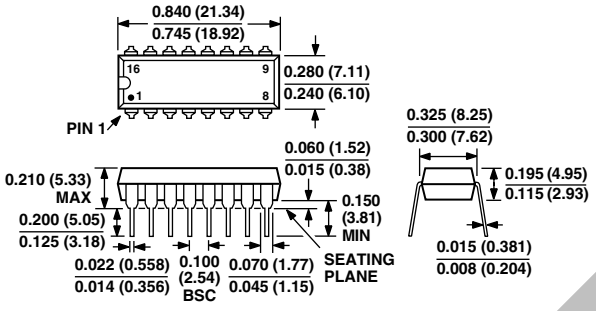
The receivers are inverting level shifters that accept EIA-232-E input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V EIA-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger input with a hysteresis level of 0.5 V. This ensures error free reception both for noisy inputs and for inputs with slow transition times.

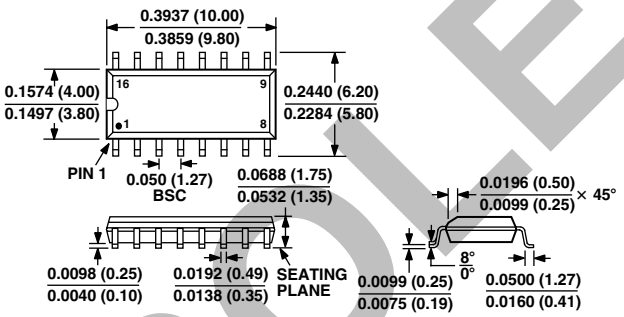
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

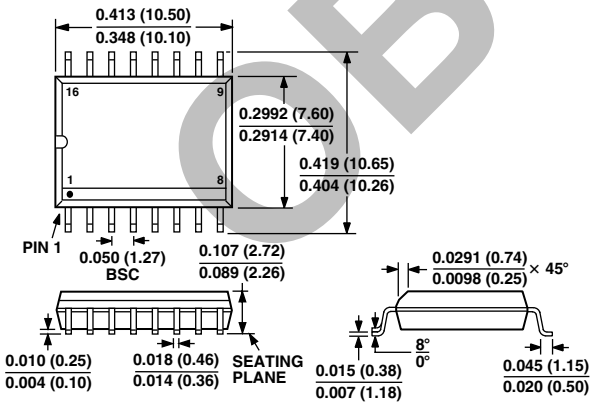
16-Lead Plastic DIP
(N-16)



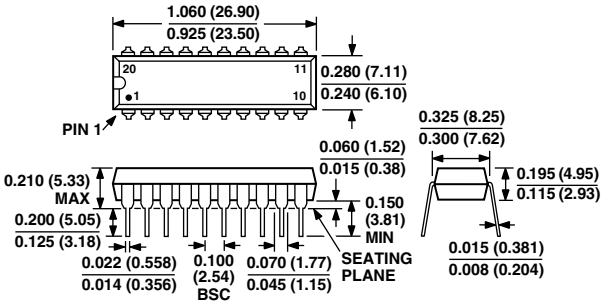
16-Lead Narrow SOIC
(R-16N)



16-Lead Wide SOIC
(R-16W)



20-Lead Plastic DIP
(N-20)



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