Ultrafast 7 ns Single Supply Comparator

AD8561

FEATURES

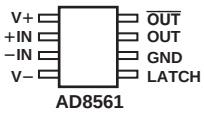
- 7 ns Propagation Delay at 5 V
- Single Supply Operation: 3 V to 10 V
- Low Power
- Latch Function
- TSSOP Packages

APPLICATIONS

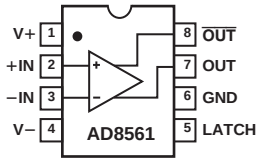
- High Speed Timing
- Clock Recovery and Clock Distribution
- Line Receivers
- Digital Communications
- Phase Detectors
- High Speed Sampling
- Read Channel Detection
- PCMCIA Cards
- Upgrade for LT1016 Designs

PIN CONFIGURATIONS

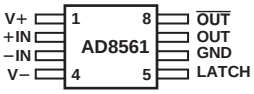
8-Lead Narrow Body SO
(SO-8)



8-Lead Plastic DIP
(N-8)



8-Lead TSSOP
(RU-8)



GENERAL DESCRIPTION

The AD8561 is a single 7 ns comparator with separate input and output sections. Separate supplies enable the input stage to be operated from ±5 V dual supplies and +5 V single supplies.

Fast 7 ns propagation delay makes the AD8561 a good choice for timing circuits and line receivers. Propagation delays for rising and falling signals are closely matched and track over temperature. This matched delay makes the AD8561 a good choice for clock recovery, since the duty cycle of the output will match the duty cycle of the input.

The AD8561 has the same pinout as the LT1016, with lower supply current and a wider common-mode input range, which includes the negative supply rail.

The AD8561 is specified over the industrial (–40°C to +85°C) temperature range. The AD8561 is available in both the 8-lead plastic DIP, 8-lead TSSOP or narrow SO-8 surface mount packages.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

AD8561–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V+ = +5.0 V, V– = V_{GND} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2.3	7	mV
		–40°C ≤ T_A ≤ +85°C			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V	–6	–3		µA
	I_B	–40°C ≤ T_A ≤ +85°C	–7	–3.5		µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±4	µA
Input Common-Mode Voltage Range	V_{CM}		0.0		+3.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT						
Logic "1" Voltage Threshold	V_{IH}		2.0	1.65		V
Logic "0" Voltage Threshold	V_{IL}			1.60	0.8	V
Logic "1" Current	I_{IH}	V_{LH} = 3.0 V	–1.0	–0.3		µA
Logic "0" Current	I_{IL}	V_{LL} = 0.3 V	–4	–2		µA
Latch Enable						
Pulsewidth	$t_{PW(E)}$			6		ns
Setup Time	t_S			1		ns
Hold Time	t_H			1.2		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = –50 µA, ΔV_{IN} > 250 mV	3.5			V
Logic "1" Voltage	V_{OH}	I_{OH} = –3.2 mA, ΔV_{IN} > 250 mV	2.4	3.5		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN} > 250 mV		0.25	0.4	V
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	200 mV Step with 100 mV Overdrive		6.75	9.8	ns
		–40°C ≤ T_A ≤ +85°C		8	13	ns
Propagation Delay	t_P	100 mV Step with 5 mV Overdrive		8		ns
Differential Propagation Delay						
(Rising Propagation Delay vs.						
Falling Propagation Delay)	Δt_P	100 mV Step with 100 mV Overdrive[1]		0.5	2.0	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		80% to 20%		1.5		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+4.5 V ≤ V+ ≤ +5.5 V	50	65		dB
Positive Supply Current	I+			4.5	6.0	mA
		–40°C ≤ T_A ≤ +85°C			7.5	mA
Ground Supply Current	I_{GND}	V_O = 0 V, R_L = ∞		2.2	3.3	mA
		–40°C ≤ T_A ≤ +85°C			3.8	mA
Analog Supply Current	I–			2.3	4.5	mA
		–40°C ≤ T_A ≤ +85°C			5.5	mA

NOTES

[1] Guaranteed by design.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V+ = +5.0 V, V– = V_{GND} = 0 V, V– = –5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	7	mV
		–40°C ≤ T_A ≤ +85°C			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0 V	–6	–3		µA
	I_B	–40°C ≤ T_A ≤ +85°C	–7	–2.5		µA
Input Offset Current	I_{OS}	V_{CM} = 0 V			±4	µA
Input Common-Mode Voltage Range	V_{CM}		–5.0		+3.0	V
Common-Mode Rejection Ratio	CMRR	–5.0 V ≤ V_{CM} ≤ +3.0 V	65	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT						
Logic "1" Voltage Threshold	V_{IH}		2.0	1.65		V
Logic "0" Voltage Threshold	V_{IL}			1.60	0.8	V
Logic "1" Current	I_{IH}	V_{LH} = 3.0 V	–1	–0.5	20	µA
Logic "0" Current	I_{IL}	V_{LL} = 0.3 V	–4	–2	20	µA
Latch Enable						
Pulsewidth	$t_{PW(E)}$			6		ns
Setup Time	t_S			1.0		ns
Hold Time	t_H			1.2		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = –3.2 mA	2.6	3.5		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA		0.2	0.3	V
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	200 mV Step with 100 mV Overdrive		6.5	9.8	ns
		–40°C ≤ T_A ≤ +85°C		8	13	ns
Propagation Delay	t_P	100 mV Step with 5 mV Overdrive		7		ns
Differential Propagation Delay (Rising Propagation Delay vs. Falling Propagation Delay)	Δt_P	100 mV Step with 100 mV Overdrive[1]		0.5	2	ns
Rise Time		20% to 80%		3.8		ns
Fall Time		80% to 20%		1.5		ns
Dispersion				1		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±4.5 V ≤ V_{CC} and V_{EE} ≤ ±5.5 V	55	70		dB
Supply Current		V_O = 0 V, R_L = ∞				
Positive Supply Current	I+			4.7	6.5	mA
		–40°C ≤ T_A ≤ +85°C			7.5	mA
Ground Supply Current	I_{GND}	V_O = 0 V, R_L = ∞		2.2	3.3	mA
		–40°C ≤ T_A ≤ +85°C			3.8	mA
Negative Supply Current	I–			2.4	4.5	mA
		–40°C ≤ T_A ≤ +85°C			5.5	mA

NOTES
[1] Guaranteed by design.

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AD8561–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V+ = +3.0 V, V– = V_{GND} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				7	mV
Input Bias Current	I_B	V_{CM} = 0 V	–6	–3.0		µA
	I_B	–40°C ≤ T_A ≤ +85°C	–7	–4		µA
Input Common-Mode Voltage Range	V_{CM}		0		+1.5	V
Common-Mode Rejection Ratio	CMRR	0.1 V ≤ V_{CM} ≤ 1.5 V	60			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = –3.2 mA, V_{IN} > 250 mV	1.2[1]			V
Output Low Voltage	V_{OL}	I_{OL} = +3.2 mA, V_{IN} > 250 mV			0.3	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+2.7 V ≤ V_{CC}, V_{EE} ≤ +6 V		40		dB
Supply Currents		V_O = 0 V, R_L = ∞				
V+ Supply Current	I+			4.0	4.5	mA
		–40°C ≤ T_A ≤ +85°C			5.5	mA
Ground Supply Current	I_{GND}			1.6	2.5	mA
		–40°C ≤ T_A ≤ +85°C			3.0	mA
V– Supply Current	I–			2.4	3.3	mA
		–40°C ≤ T_A ≤ +85°C			3.8	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t_P	100 mV Step with 20 mV Overdrive[2]		8.5	9.8	ns

NOTES
[1]Output high voltage without pull-up resistor. It may be useful to have a pull-up resistor to V+ for 3 V operation.
[2]Guaranteed by design.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Analog Supply Voltage . . . . . +14 V
Digital Supply Voltage . . . . . +14 V
Analog Positive Supply–Digital Positive Supply . . . . . –600 mV
Input Voltage[1] . . . . . ±7 V
Differential Input Voltage . . . . . ±8 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
N, R, RU Package . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range
N, R, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +350°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Lead Plastic DIP (N)	103	43	°C/W
8-Lead SO (R)	158	43	°C/W
8-Lead TSSOP	240	43	°C/W

NOTES
[1]The analog input voltage is equal to ±7 V or the analog supply voltage, whichever is less.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8561 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Characteristics (V+ = +5 V, V– = 0 V, T_A = +25°C unless otherwise noted)

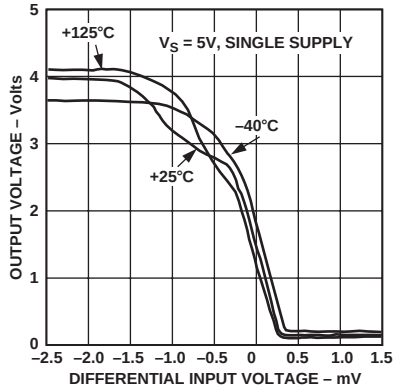


Figure 1. Output Voltage vs. Differential Input Voltage

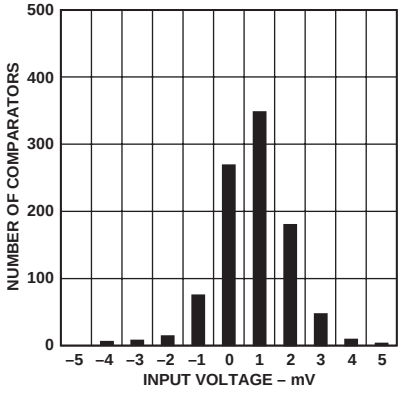


Figure 2. Typical Distribution of Input Offset Voltage

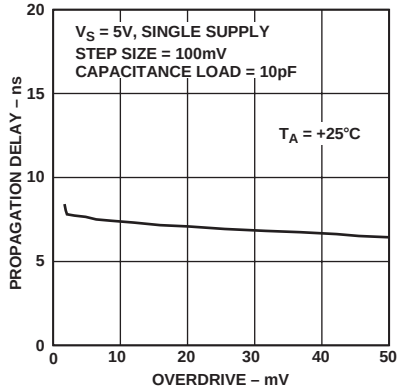


Figure 3. Propagation Delay vs. Overdrive

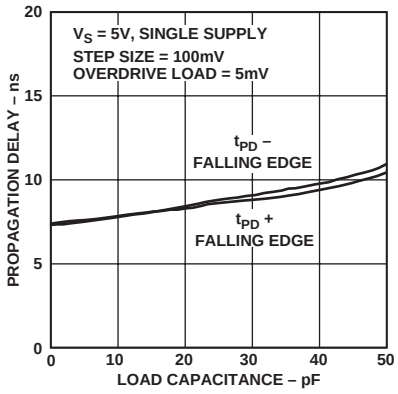


Figure 4. Propagation Delay vs. Load Capacitance

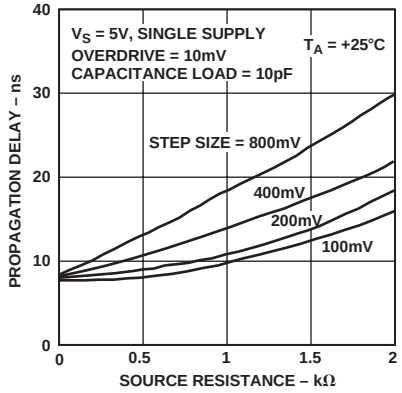


Figure 5. Propagation Delay vs. Source Resistance

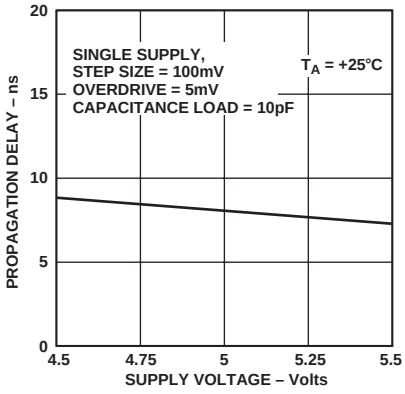


Figure 6. Propagation Delay vs. Positive Supply Voltage

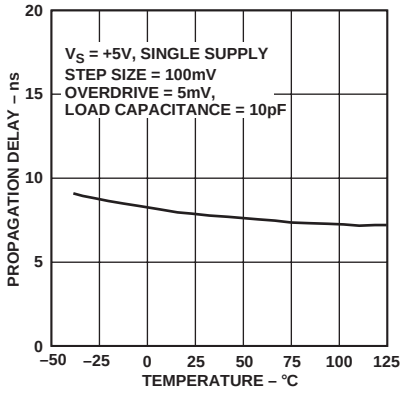


Figure 7. Propagation Delay vs. Temperature

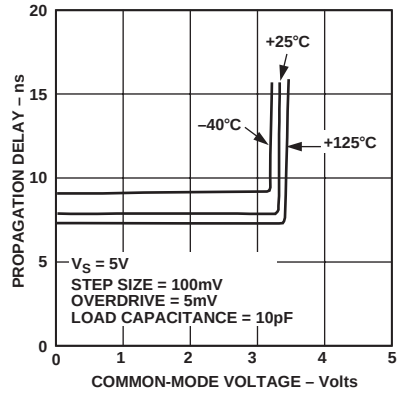


Figure 8. Propagation Delay vs. V_{CM}

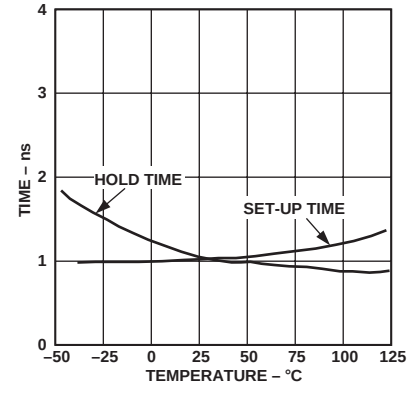


Figure 9. Latch Setup-and-Hold Time vs. Temperature

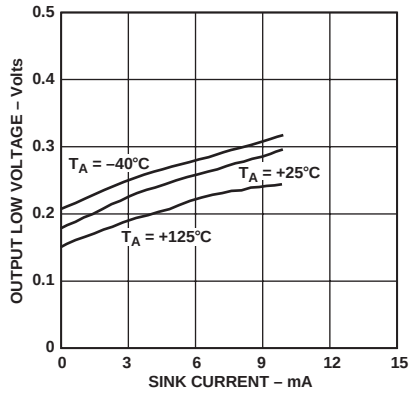


Figure 10. Output Low Voltage, V_{OL} vs. Sink Current

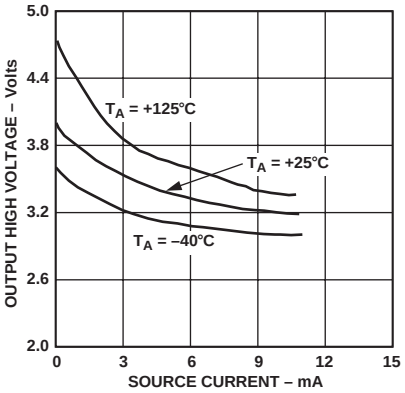


Figure 11. Output High Voltage, V_{OH} vs. Source Current

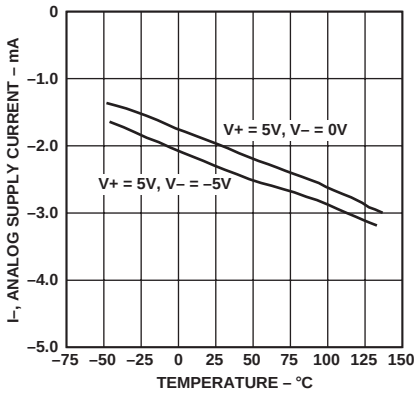


Figure 12. Analog Supply Current vs. Temperature for +5 V, –5 V Supplies

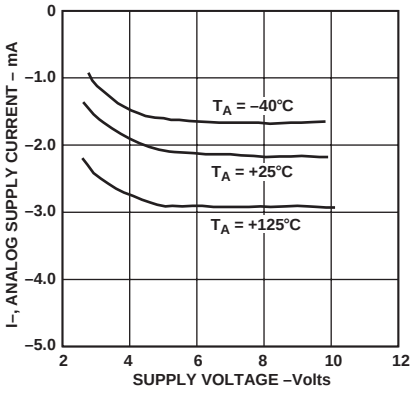


Figure 13. Analog Supply Current vs. Supply Voltage for +5 V, –5 V Supplies

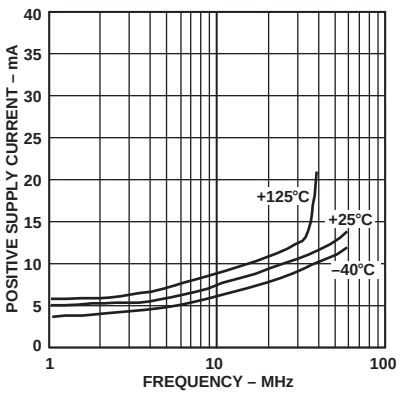


Figure 14. Positive Supply Current vs. Frequency

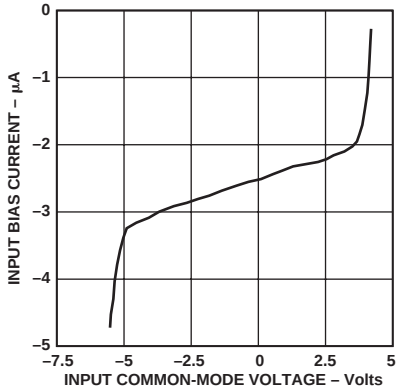


Figure 15. Input Bias Current vs. Input Common-Mode Voltage for +5 V, –5 V Supplies

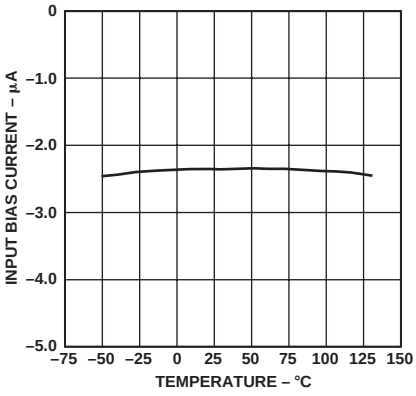


Figure 16. Input Bias Current vs. Temperature

APPLICATIONS

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator or amplifier, proper design and layout techniques should be used to ensure optimal performance from the AD8561. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the AD8561. Source resistance in combination with equivalent input capacitance could cause a lagged response at the input, thus delaying the output. The input capacitance of the AD8561 in combination with stray capacitance from an input pin to ground could result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF of input capacitance yields a time constant of 15 ns, which is slower than the 5 ns capability of the AD8561. Source impedances should be less than 1 kΩ for the best performance.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1 μF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin, Pin 1 and Pin 4, to ground. These capacitors will reduce any potential voltage ripples from the power supply. In addition, a 10 nF ceramic capacitor should be placed as close as possible from the power supply pins to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

A ground plane is recommended for proper high speed performance. This can be created by using a continuous conductive plane over the surface of the circuit board, only allowing breaks in the plane for necessary current paths. The ground plane provides a low inductive ground, eliminating any potential differences at different ground points throughout the circuit board caused from "ground bounce." A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

REPLACING THE LT1016

The AD8561 is pin compatible with the LT1016 comparator. While it is easy to replace the LT1016 with the higher performance AD8561, please note that there are differences, and it is useful to check these to ensure proper operation.

There are five major differences between the AD8561 and the LT1016—input voltage range, input bias currents, speed, output swing and power consumption.

When operated on a +5 V single supply, the LT1016 has an input voltage range from +1.25 V to +3.5 V. The AD8561 has a wider input range from 0 V to 3.0 V. Signals above 3.0 V may result in slower response times (see Figure 8). If both signals exceed 3.0 V, the signals may be shifted or attenuated to bring them into range, keeping in mind the note about source resistance in Optimizing High Speed Performance. If only one of the signals exceeds 3.0 V only slightly, and the other signal is always well within the 0 V to 3 V range, the comparator may operate without changes to the circuit.

Example: A comparator compares a fast moving signal to a fixed 2.5 V reference. Since the comparator only needs to operate when the signal is near 2.5 V, both signals will be within the input range (near 2.5 V and well under 3.0 V) when the comparator needs to change output.

Note that signals much greater than 3.0 V will result increased input currents and may cause the device to operate more slowly.

The input bias current of the AD8561 is lower (–3 μA typical) than the LT1016 (+5 μA typical), and the current flows out of the AD8561 and into LT1016. If relatively low value resistors and/or low impedance sources are used on the inputs, the voltage shift due to bias current should be small.

The AD8561 (6.75 ns typical) is faster than the LT1016 (10 ns typical). While this is beneficial to many systems, timing may need to be adjusted to take advantage of the higher speed.

The AD8561 has slightly more output voltage swing, from 0.2 V above ground to within 1.1 V of the positive supply voltage.

The AD8561 uses less current (typically 5 mA) than the LT1016 (typically 25 mA).

INCREASING OUTPUT SWING

Although not required for normal operation, the output voltage swing of the AD8561 can be increased by connecting a 5 kΩ resistor from the output of the device to the V+ power supply. This configuration can be useful in low voltage power supply applications where maximizing output voltage swing is important. Adding a 5 kΩ pull-up resistor to the device's output will not adversely affect the specifications of the AD8561.

OUTPUT LOADING CONSIDERATIONS

The AD8561 output can deliver up to 40 mA of output current without any significant increase in propagation delay. The output of the device should not be connected to more than twenty (20) TTL input logic gates, or drive a load resistance less than 100 Ω.

To ensure the best performance from the AD8561 it is important to minimize capacitive loading of the output of the device. Capacitive loads greater than 50 pF will cause ringing on the output waveform and will reduce the operating bandwidth of the comparator.

SETUP AND HOLD TIMES FOR LATCHING THE OUTPUT

The latch input, Pin 5, can be used to retain data at the output of the AD8561. When the voltage at the latch input goes high, the output of the device will remain constant regardless of the input voltages. The setup time for the latch is 2 ns–3 ns and the hold time is 3 ns. This means that to ensure data retention at the output, the input signal must be valid at least 5 ns before the latch pin goes high and must remain valid at least 3 ns after the latch pin goes high. Once the latch input voltage goes low, new output data will appear in approximately 8 ns.

A logic high for the latch input is a minimum of +2.0 V and a logic low is a maximum of +0.8 V. This makes the latch input easily interface with TTL or CMOS logic gates. The latch circuitry in the AD8561 has no built-in hysteresis.

INPUT STAGE AND BIAS CURRENTS

The AD8561 uses a PNP differential input stage that enables the input common-mode range to extend all the way from the negative supply rail to within 2.2 V of the positive supply rail. The input common-mode voltage can be found as the average of the voltage at the two inputs of the device. To ensure the fastest response time, care should be taken not to allow the input common-mode voltage to exceed either of these voltages.

The input bias current for the AD8561 is 3 μA. As with any PNP differential input stage, this bias current will go to zero on an input that is high and will double on an input that is low. Care should be taken in choosing resistor values to be connected to the inputs as large resistors could cause significant voltage drops due to the input bias current.

The input capacitance for the AD8561 is typically 3 pF. This is measured by inserting a 5 kΩ source resistance to the input and measuring the change in propagation delay.

USING HYSTERESIS

Hysteresis can easily be added to a comparator through the addition of positive feedback. Adding hysteresis to a comparator offers an advantage in noisy environments where it is not desirable for the output to toggle between states when the input signal is near the switching threshold. Figure 17 shows a method for configuring the AD8561 with hysteresis.

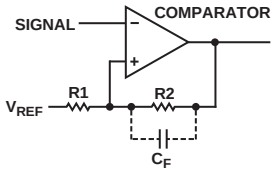


Figure 17. Configuring the AD8561 with Hysteresis

The input signal is connected directly to the noninverting input of the comparator. The output is fed back to the inverting input through R1 and R2. The ratio of R1 to R1 + R2 establishes the width of the hysteresis window with V_{REF} setting the center of the window, or the average switching voltage. The Q output will switch high when the input voltage is greater than V_{HI} and will not switch low again until the input voltage is less than V_{LO} as given in Equation 1:

$$V_{HI} = \left(V_+ - 1 - V_{REF}\right)\frac{R1}{R1+R2} + V_{REF}$$

$$V_{LO} = V_{REF}\left(1 - \frac{R1}{R1+R2}\right) \quad (1)$$

Where V_+ is the positive supply voltage.

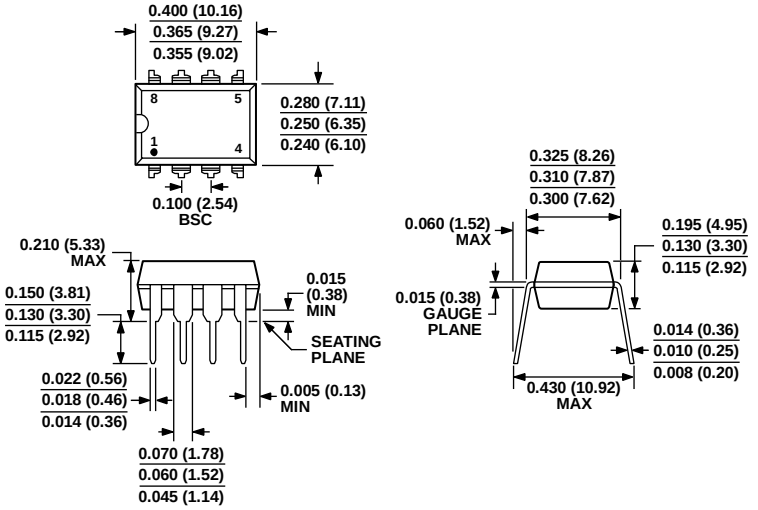
The capacitor C_F can also be added to introduce a pole into the feedback network. This has the effect of increasing the amount of hysteresis at high frequencies. This can be useful when comparing a relatively slow signal in a high frequency noise environment. At frequencies greater than $f_P = \frac{1}{2\pi C_F R2}$, the hysteresis window approaches $V_{HI} = V_+ - 1$ V and $V_{LO} = 0$ V. At frequencies less than f_P the threshold voltages remain as in Equation 1.

SPICE Model

```
* AD8561 SPICE Macro-Model Typical Values
* 4/98, Ver. 1.0
* TAM / ADSC
*
* Node assignments
*                 non-inverting input
*                 |        inverting input
*                 |        |        positive supply
*                 |        |        |        negative supply
*                 |        |        |        |        Latch
*                 |        |        |        |        |        DGND
*                 |        |        |        |        |        |        Q
*                 |        |        |        |        |        |        |        QNOT
*                 |        |        |        |        |        |        |        |
.SUBCKT AD8561    1        2        99       50       80       51       45       65
*
* INPUT STAGE
*
*
Q1      4   3 5 PIX
Q2      6   2 5 PIX
IBIAS 99   5 800E-6
RC1     4 50 1E3
RC2     6 50 1E3
CL1     4   6 1E-12
CIN     1   2 3E-12
VCM1   99   7 1
D1      5   7 DX
EOS     3   1 POLY(1) (31,98) 1E-3 1
*
* Reference Voltage
*
EREF 98 0 POLY(2) (99,0) (50,0) 0 0.5 0.5
RREF 98 0 100E3
*
* CMRR=80dB, ZERO AT 1kHz
*
ECM1 30 98 POLY(2) (1,98) (2,98) 0 0.5 0.5
RCM1 30 31 10E3
RCM2 31 98 1
CCM1 30 31 15.9E-9
*
* Latch Section
*
RX 80 51 100E3
E1 10 98 (4,6) 1
S1 10 11 (80,51) SLATCH1
R2 11 12 1
C3 12 98 10E-12
E2 13 98 (12,98) 1
R3 12 13 500
*
* Power Supply Section
*
```

```
GSY1 99 52 POLY(1) (99,50) 4E-3 -2.6E-4
GSY2 52 50 POLY(1) (99,50) 3.7E-3 -.6E-3
RSY  52 51 10
*
* Gain Stage Av=250 fp=100MHz
*
G2 98 20 (12,98) 0.25
R1 20 98 1000
C1 20 98 10E-13
D2 20 21 DX
D3 22 20 DX
V1 99 21 DC 0.8
V2 22 50 DC 0.8
*
* Q Output
*
Q3  99 41 46 NOX
Q4  47 42 50 NOX
RB1 43 41 200
RB2 40 42 5E3
CB1 99 41 10E-12
CB2 42 50 5E-12
RO1 46 45 2E3
RO2 47 45 500
EO1 98 43 POLY(1) (20,98) 0 1
EO2 40 98 POLY(1) (20,98) 0 1
*
* Q NOT Output
*
Q5  99 61 66 NOX
Q6  67 62 50 NOX
RB3 63 61 200
RB4 60 62 5E3
CB3 99 61 10E-12
CB4 62 50 5E-12
RO3 66 65 2E3
RO4 67 65 500
EO3 63 98 POLY(1) (20,98) 0 1
EO4 98 60 POLY(1) (20,98) 0 1
*
* MODELS
*
.MODEL PIX PNP(BF=100,IS=1E-16)
.MODEL NOX NPN(BF=100,VAF=130,IS=1E-14)
.MODEL DX D(IS=1E-16)
.MODEL SLATCH1 VSWITCH(ROFF=1E6,RON=500,VOFF=2.1,VON=1.4)
.ENDS AD8561
```

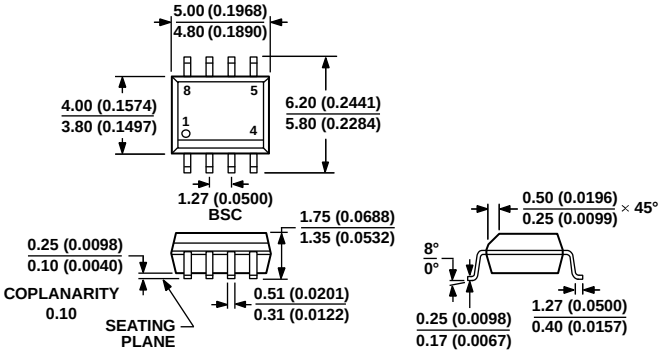
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

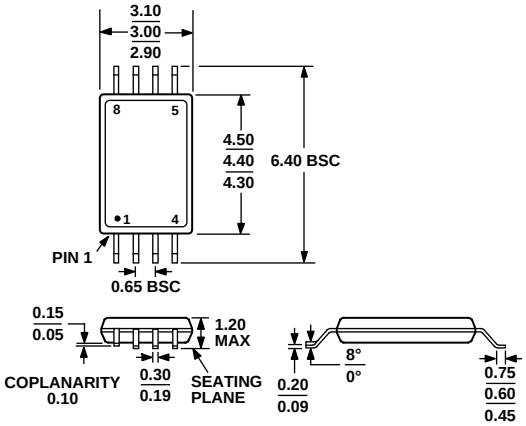
070606-A

Figure 18. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-8)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 19. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AA

Figure 20. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body(R-8)
Dimensions shown in millimeters and (inches

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8561ANZ	−40°C to +85°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD8561ARUZ	−40°C to +85°C	8-Lead Thin Shrink Small Outline Package [TSSOP]	RU-8
AD8561ARUZ-REEL	−40°C to +85°C	8-Lead Thin Shrink Small Outline Package [TSSOP]	RU-8
AD8561ARZ	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	SO-8
AD8561ARZ-REEL	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	SO-8
AD8561ARZ-REEL7	−40°C to +85°C	8-Lead Standard Small Outline Package [SOIC_N]	SO-8

[1] Z = RoHS Compliant Part.

REVISION HISTORY

5/13—Rev. 0 to Rev. A

Change to Lead Temperature Range (Soldering, 10 Sec) Parameter, Absolute Maximum Ratings Section 4
Updated Outline Dimensions 11
Moved Ordering Guide and Added Revision History Section 12
Changes to Ordering Guide 12

6/98—Revision 0: Initial Version

D3220-0-5/13(A)