# MC14016B

# Quad Analog Switch/ Quad Multiplexer

The MC14016B quad bilateral switch is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each MC14016B consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

### Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise − 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- Pin−for−Pin Replacements for CD4016B, CD4066B (Note improved transfer characteristic design causes more parasitic coupling capacitance than CD4016)
- For Lower $R_{ON}$, Use The HC4016 High−Speed CMOS Device or The MC14066B
- This Device Has Inputs and Outputs Which Do Not Have ESD Protection. Antistatic Precautions Must Be Taken
- These Devices are Pb−Free and are RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | Input Current (DC or Transient) per Control Pin | ±10 | mA |
| $I_{SW}$ | Switch Through Current | ±25 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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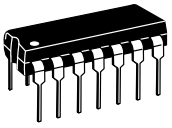
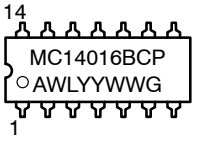
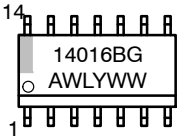
**MARKING DIAGRAMS**

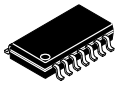


**PDIP−14**
**P SUFFIX**
**CASE 646**



**SOIC−14**
**D SUFFIX**
**CASE 751A**



**SOEIAJ−14**
**F SUFFIX**
**CASE 965**

| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G | = Pb−Free Indicator |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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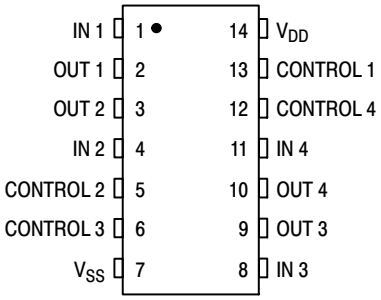
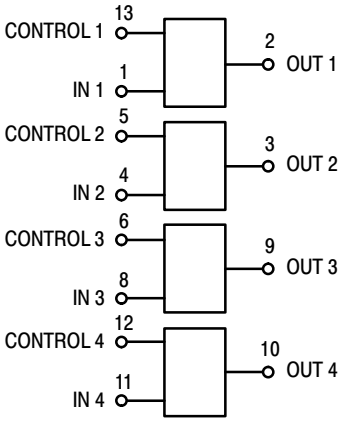
### PIN ASSIGNMENT



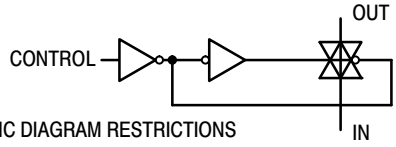

### BLOCK DIAGRAM




$V_{DD}$ = PIN 14
$V_{SS}$ = PIN 7

### LOGIC DIAGRAM

(1/4 OF DEVICE SHOWN)




LOGIC DIAGRAM RESTRICTIONS
$V_{SS} \le V_{in} \le V_{DD}$
$V_{SS} \le V_{out} \le V_{DD}$

| Control | Switch |
|---|---|
| 0 = $V_{SS}$ | Off |
| 1 = $V_{DD}$ | On |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14016BCPG | PDIP−14<br>(Pb−Free) | 500 / Tube |
| MC14016BDG | SOIC−14<br>(Pb−Free) | 55 Units / Rail |
| MC14016BDR2G | SOIC−14<br>(Pb−Free) | 2500 / Tape & Reel |
| MC14016BFELG | SOEIAJ−14<br>(Pb−Free) | 2000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Figure | Symbol | $V_{DD}$ Vdc | – 55°C Min | – 55°C Max | 25°C Min | 25°C Typ (2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Voltage<br>Control Input | 1 | $V_{IL}$ | 5.0<br>10<br>15 | –<br>–<br>– | –<br>–<br>– | –<br>–<br>– | 1.5<br>1.5<br>1.5 | 0.9<br>0.9<br>0.9 | –<br>–<br>– | –<br>–<br>– | Vdc |
| | | $V_{IH}$ | 5.0<br>10<br>15 | –<br>–<br>– | –<br>–<br>– | 3.0<br>8.0<br>13 | 2.0<br>6.0<br>11 | –<br>–<br>– | –<br>–<br>– | –<br>–<br>– | Vdc |
| Input Current Control | – | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ± 1.0 | μAdc |
| Input Capacitance<br>Control<br>Switch Input<br>Switch Output<br>Feed Through | – | $C_{in}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>5.0<br>5.0<br>5.0<br>0.2 | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | pF |
| Quiescent Current<br>(Per Package) (3) | 2,3 | $I_{DD}$ | 5.0<br>10<br>15 | –<br>–<br>– | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 0.0005<br>0.0010<br>0.0015 | 0.25<br>0.5<br>1.0 | –<br>–<br>– | 7.5<br>15<br>30 | μAdc |
| "ON" Resistance<br>($V_C = V_{DD}$, $R_L$ = 10 kΩ)<br>($V_{in}$ = + 10 Vdc)<br>($V_{in}$ = + 0.25 Vdc) $V_{SS}$ = 0 Vdc<br>($V_{in}$ = + 5.6 Vdc)<br>($V_{in}$ = + 15 Vdc)<br>($V_{in}$ = + 0.25 Vdc) $V_{SS}$ = 0 Vdc<br>($V_{in}$ = + 9.3 Vdc) | 4,5,6 | $R_{ON}$ | <br><br><br>10<br><br><br>15 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>600<br>600<br>600<br>360<br>360<br>360 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>260<br>310<br>310<br>260<br>260<br>300 | <br>660<br>660<br>660<br>400<br>400<br>400 | <br>–<br>–<br>–<br>–<br>–<br>–<br>– | <br>840<br>840<br>840<br>520<br>520<br>520 | Ω |
| Δ "ON" Resistance<br>Between any 2 circuits in a common package<br>($V_C = V_{DD}$)<br>($V_{in}$ = + 5.0 Vdc, $V_{SS}$ = – 5.0 Vdc)<br>($V_{in}$ = + 7.5 Vdc, $V_{SS}$ = – 7.5 Vdc) | – | $\Delta R_{ON}$ | <br><br><br>5.0<br>7.5 | <br><br><br>–<br>– | <br><br><br>–<br>– | <br><br><br>–<br>– | <br><br><br>15<br>10 | <br><br><br>–<br>– | <br><br><br>–<br>– | <br><br><br>–<br>– | Ω |
| Input/Output Leakage Current<br>($V_C = V_{SS}$)<br>($V_{in}$ = + 7.5, $V_{out}$ = – 7.5 Vdc)<br>($V_{in}$ = – 7.5, $V_{out}$ = + 7.5 Vdc) | – | – | <br>7.5<br>7.5 | <br>–<br>– | <br>±0.1<br>±0.1 | <br>–<br>– | <br>±0.0015<br>±0.0015 | <br>±0.1<br>± 0.1 | <br>–<br>– | <br>± 1.0<br>± 1.0 | μAdc |

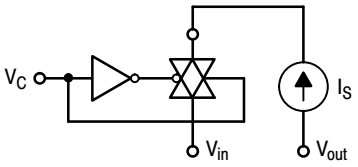
NOTE: All unused inputs must be returned to $V_{DD}$ or $V_{SS}$ as appropriate for the circuit application.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. For voltage drops across the switch ($\Delta V_{switch}$) > 600 mV ( > 300 mV at high temperature), excessive $V_{DD}$ current may be drawn; i.e., the current out of the switch may contain both $V_{DD}$ and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.) Reference Figure 14.

**ELECTRICAL CHARACTERISTICS** [4] ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Figure | Symbol | $V_{DD}$ Vdc | Min | Typ [5] | Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time ($V_{SS}$ = 0 Vdc)<br>$V_{in}$ to $V_{out}$<br>($V_C$ = $V_{DD}$, $R_L$ = 10 kΩ) | 7 | $t_{PLH}$,<br>$t_{PHL}$ | 5.0<br>10<br>15 | –<br>–<br>– | 15<br>7.0<br>6.0 | 45<br>20<br>15 | ns |
| Control to Output<br>($V_{in}$ ≤ 10 Vdc, $R_L$ = 10 kΩ) | 8 | $t_{PHZ}$,<br>$t_{PLZ}$,<br>$t_{PZH}$,<br>$t_{PZL}$ | <br>5.0<br>10<br>15 | <br>–<br>–<br>– | <br>34<br>20<br>15 | <br>120<br>110<br>100 | ns |
| Crosstalk, Control to Output ($V_{SS}$ = 0 Vdc)<br>($V_C$ = $V_{DD}$, $R_{in}$ = 10 kΩ, $R_{out}$ = 10 kΩ,<br>f = 1.0 kHz) | 9 | – | 5.0<br>10<br>15 | –<br>–<br>– | 30<br>50<br>100 | –<br>–<br>– | mV |
| Crosstalk between any two switches ($V_{SS}$ = 0 Vdc)<br>($R_L$ = 1.0 kΩ, f = 1.0 MHz,<br>crosstalk = $20\log_{10}\frac{V_{out1}}{V_{out2}}$) | – | – | 5.0 | – | −80 | – | dB |
| Noise Voltage ($V_{SS}$ = 0 Vdc)<br>($V_C$ = $V_{DD}$, f = 100 Hz)<br><br>($V_C$ = $V_{DD}$, f = 100 kHz) | 10,11 | – | 5.0<br>10<br>15<br><br>5.0<br>10<br>15 | –<br>–<br>–<br><br>–<br>–<br>– | 24<br>25<br>30<br><br>12<br>12<br>15 | –<br>–<br>–<br><br>–<br>–<br>– | nV/$\sqrt{\text{Cycle}}$ |
| Second Harmonic Distortion ($V_{SS}$ = − 5.0 Vdc)<br>($V_{in}$ = 1.77 Vdc, RMS Centered @ 0.0 Vdc,<br>$R_L$ = 10 kΩ, f = 1.0 kHz) | – | – | 5.0 | – | 0.16 | – | % |
| Insertion Loss ($V_C$ = $V_{DD}$, $V_{in}$ = 1.77 Vdc,<br>$V_{SS}$ = − 5.0 Vdc, RMS centered = 0.0 Vdc, f = 1.0 MHz)<br>$I_{loss}$ = $20\log_{10}\frac{V_{out}}{V_{in}}$)<br>($R_L$ = 1.0 kΩ)<br>($R_L$ = 10 kΩ)<br>($R_L$ = 100 kΩ)<br>($R_L$ = 1.0 MΩ) | 12 | – | 5.0 | <br><br>–<br>–<br>–<br>– | <br><br>2.3<br>0.2<br>0.1<br>0.05 | <br><br>–<br>–<br>–<br>– | dB |
| Bandwidth (− 3.0 dB)<br>($V_C$ = $V_{DD}$, $V_{in}$ = 1.77 Vdc, $V_{SS}$ = − 5.0 Vdc,<br>RMS centered @ 0.0 Vdc)<br>($R_L$ = 1.0 kΩ)<br>($R_L$ = 10 kΩ)<br>($R_L$ = 100 kΩ)<br>($R_L$ = 1.0 MΩ) | 12,13 | BW | 5.0 | <br><br>–<br>–<br>–<br>– | <br><br>54<br>40<br>38<br>37 | <br><br>–<br>–<br>–<br>– | MHz |
| OFF Channel Feedthrough Attenuation<br>($V_{SS}$ = − 5.0 Vdc)<br>($V_C$ = $V_{SS}$, 20 $\log_{10}\frac{V_{out}}{V_{in}}$ = −50 dB)<br>($R_L$ = 1.0 kΩ)<br>($R_L$ = 10 kΩ)<br>($R_L$ = 100 kΩ)<br>($R_L$ = 1.0 MΩ) | – | – | 5.0 | <br><br>–<br>–<br>–<br>– | <br><br>1250<br>140<br>18<br>2.0 | <br><br>–<br>–<br>–<br>– | kHz |

4. The formulas given are for typical characteristics only at 25°C.
5. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.




$V_{IL}$: $V_C$ is raised from $V_{SS}$ until $V_C = V_{IL}$.
at $V_C = V_{IL}$: $I_S = \pm 10$ μA with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

$V_{IH}$: When $V_C = V_{IH}$ to $V_{DD}$, the switch is ON and the $R_{ON}$ specifications are met.

**Figure 1. Input Voltage Test Circuit**

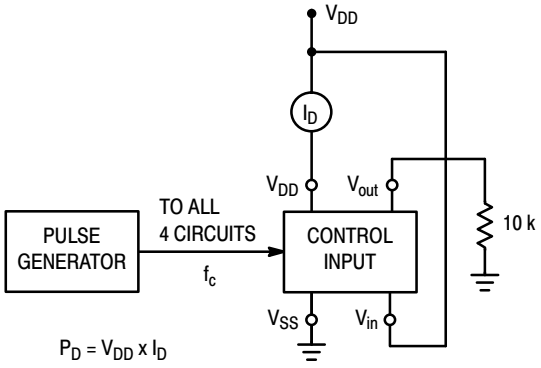



**Figure 2. Quiescent Power Dissipation Test Circuit**

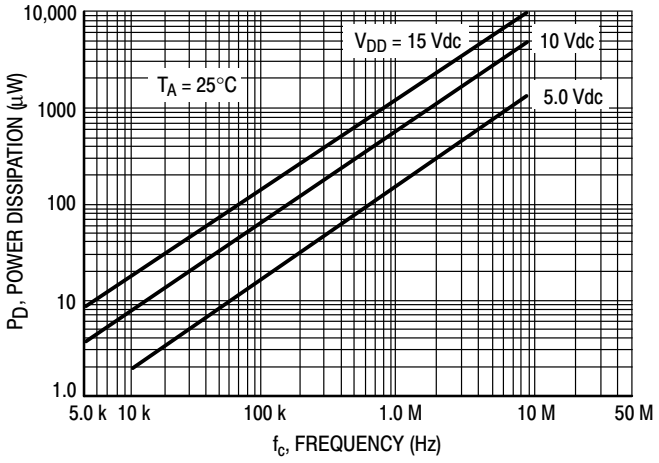



**Figure 3. Typical Power Dissipation per Circuit (1/4 of device shown)**

## TYPICAL $R_{ON}$ versus INPUT VOLTAGE

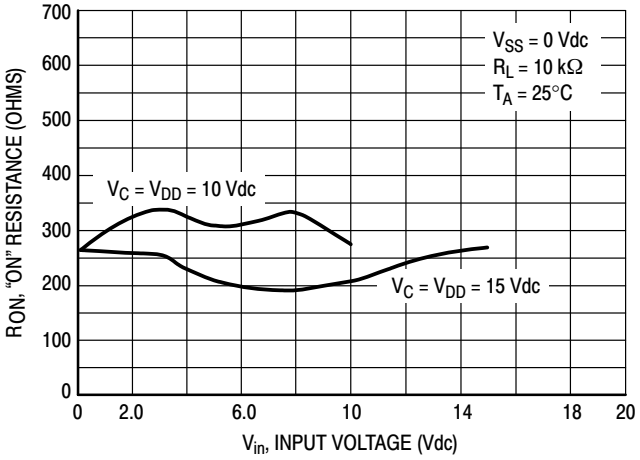



**Figure 4. $V_{SS}$ = 0 V**

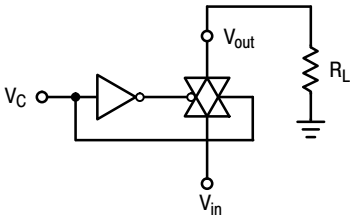



**Figure 5. $R_{ON}$ Characteristics Test Circuit**

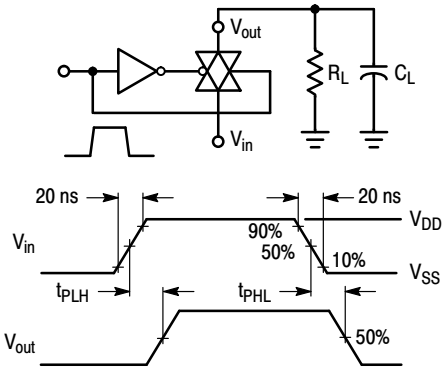



**Figure 6. Propagation Delay Test Circuit and Waveforms**

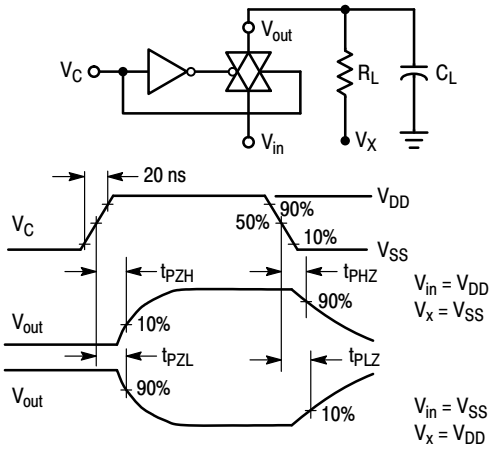



**Figure 7. Turn–On Delay Time Test Circuit and Waveforms**

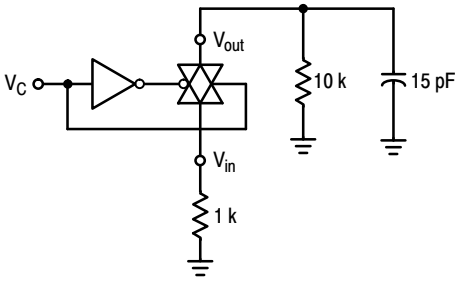



**Figure 8. Crosstalk Test Circuit**

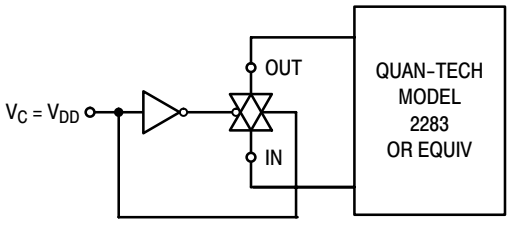



**Figure 9. Noise Voltage Test Circuit**

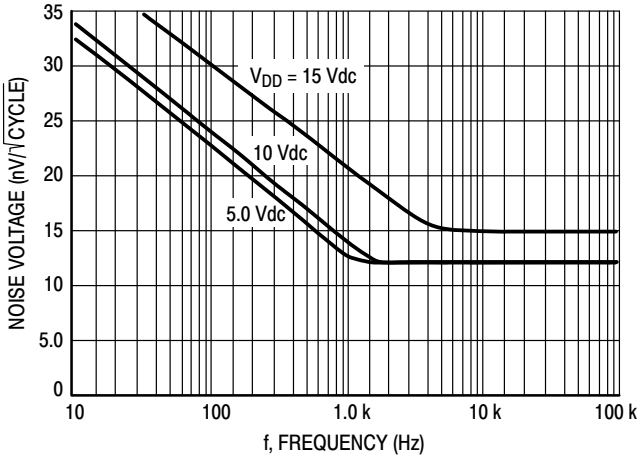



**Figure 10. Typical Noise Characteristics**

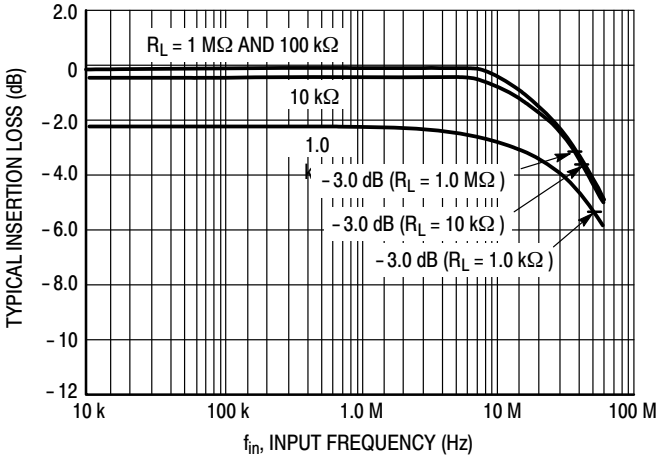



**Figure 11. Typical Insertion Loss/Bandwidth Characteristics**

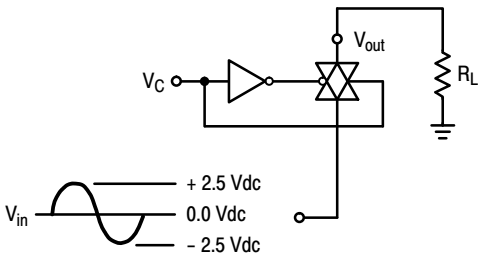



**Figure 12. Frequency Response Test Circuit**

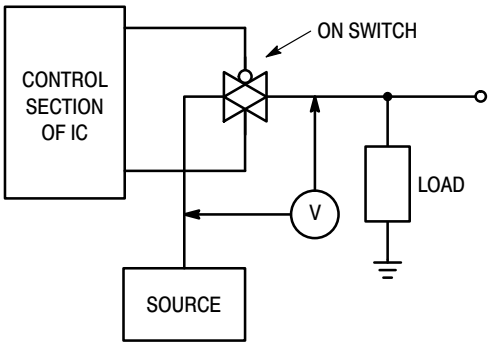



**Figure 13. ΔV Across Switch**

## APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0–to–5 V Digital Control signal is used to directly control a 5 $V_{p-p}$ analog signal.

The digital control logic levels are determined by $V_{DD}$ and $V_{SS}$. The $V_{DD}$ voltage is the logic high voltage; the $V_{SS}$ voltage is logic low. For the example, $V_{DD}$ = +5 V logic high at the control inputs; $V_{SS}$ = GND = 0 V logic low.

The maximum analog signal level is determined by $V_{DD}$ and $V_{SS}$. The analog voltage must not swing higher than $V_{DD}$ or lower than $V_{SS}$.

The example shows a 5 $V_{p-p}$ signal which allows no margin at either peak. If voltage transients above $V_{DD}$ and/or below $V_{SS}$ are anticipated on the analog channels, external diodes ($D_x$) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between $V_{DD}$ and $V_{SS}$ is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between $V_{DD}$ and $V_{SS}$.

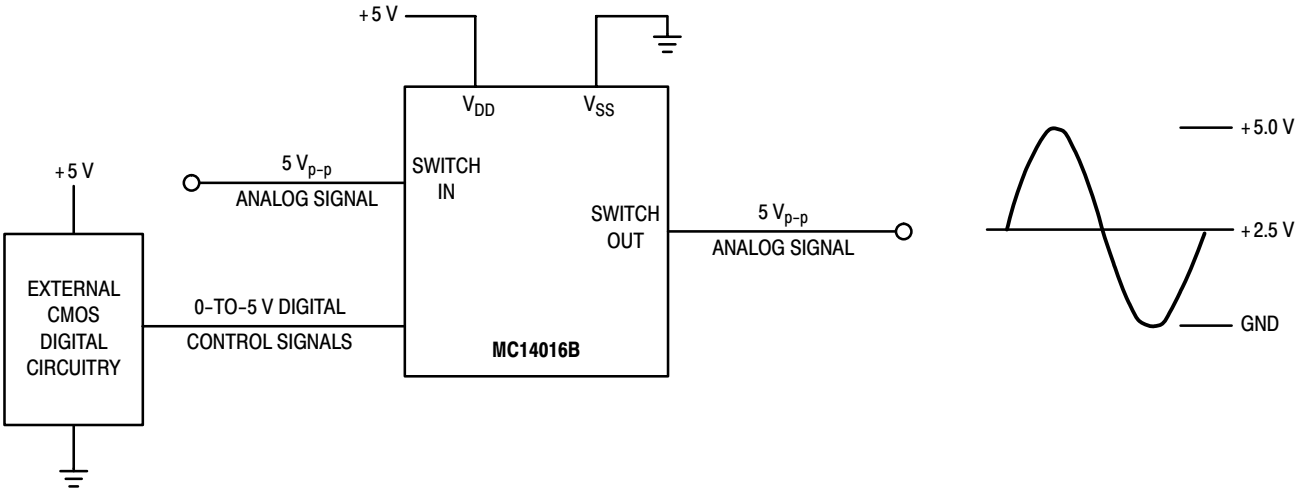



**Figure A. Application Example**

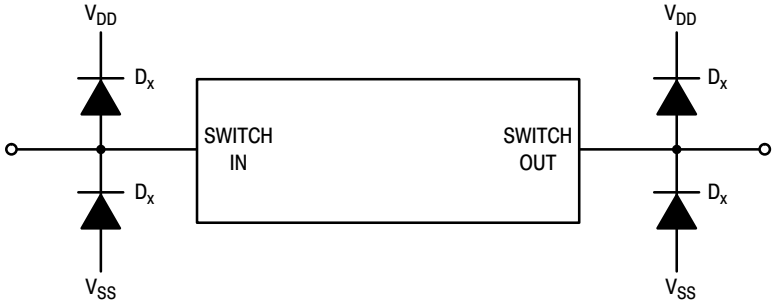
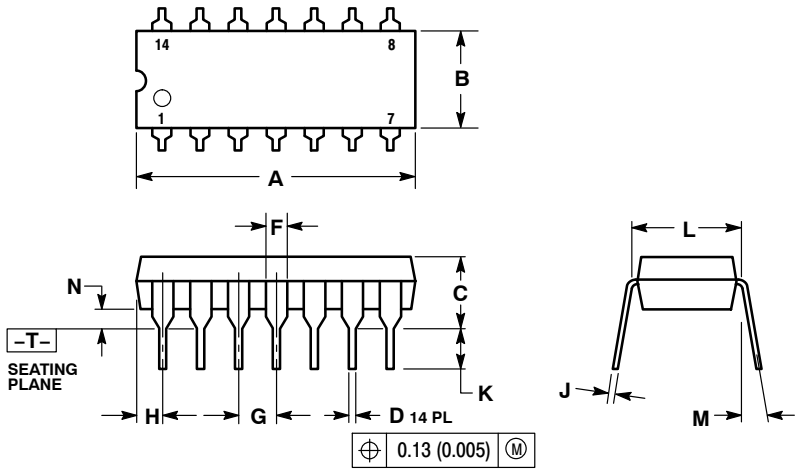



**Figure B. External Germanium or Schottky Clipping Diodes**

## PACKAGE DIMENSIONS

**PDIP−14**
CASE 646−06
ISSUE P

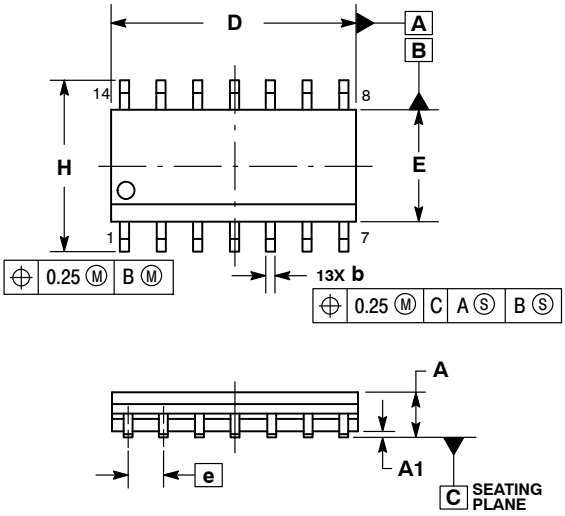


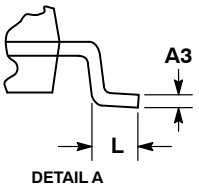

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

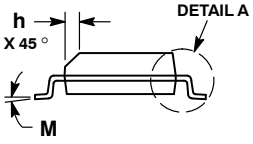
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.290 | 0.310 | 7.37 | 7.87 |
| M | −−− | 10 ° | −−− | 10 ° |
| N | 0.015 | 0.039 | 0.38 | 1.01 |

## PACKAGE DIMENSIONS

**SOIC−14 NB**
CASE 751A−03
ISSUE K



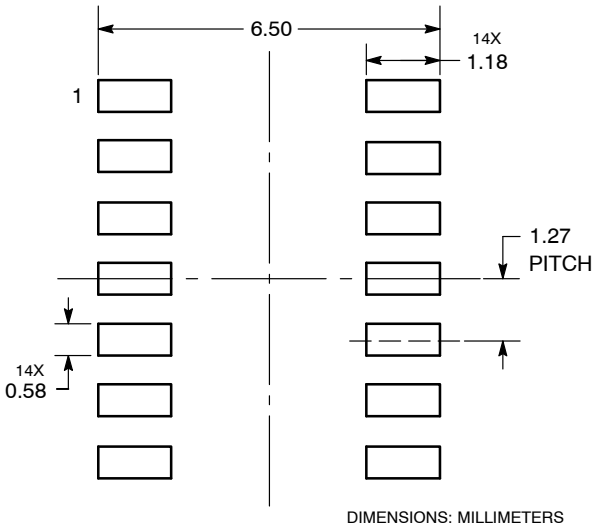




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |

### SOLDERING FOOTPRINT*

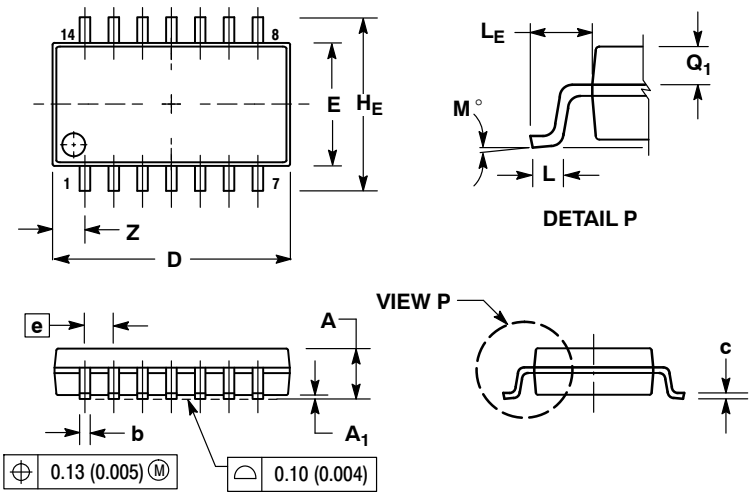



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**SOEIAJ−14**
CASE 965−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| $A_1$ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.10 | 0.20 | 0.004 | 0.008 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| $H_E$ | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| $L_E$ | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| $Q_1$ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 1.42 | --- | 0.056 |

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