

74LVC245A; 74LVCH245A

Octal bus transceiver; 3-state

Rev. 9 — 11 September 2018

Product data sheet

1. General description

The 74LVC245A; 74LVCH245A are 8-bit transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features an output enable (\overline{OE}) input for easy cascading and a send/receive (DIR) input for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH245A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{CC} = 0$ V
- Bus hold on all data inputs (74LVCH245A only)
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC245AD	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVCH245AD				
74LVC245ADB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVCH245ADB				
74LVC245APW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVCH245APW				
74LVC245ABQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1
74LVCH245ABQ				

4. Functional diagram

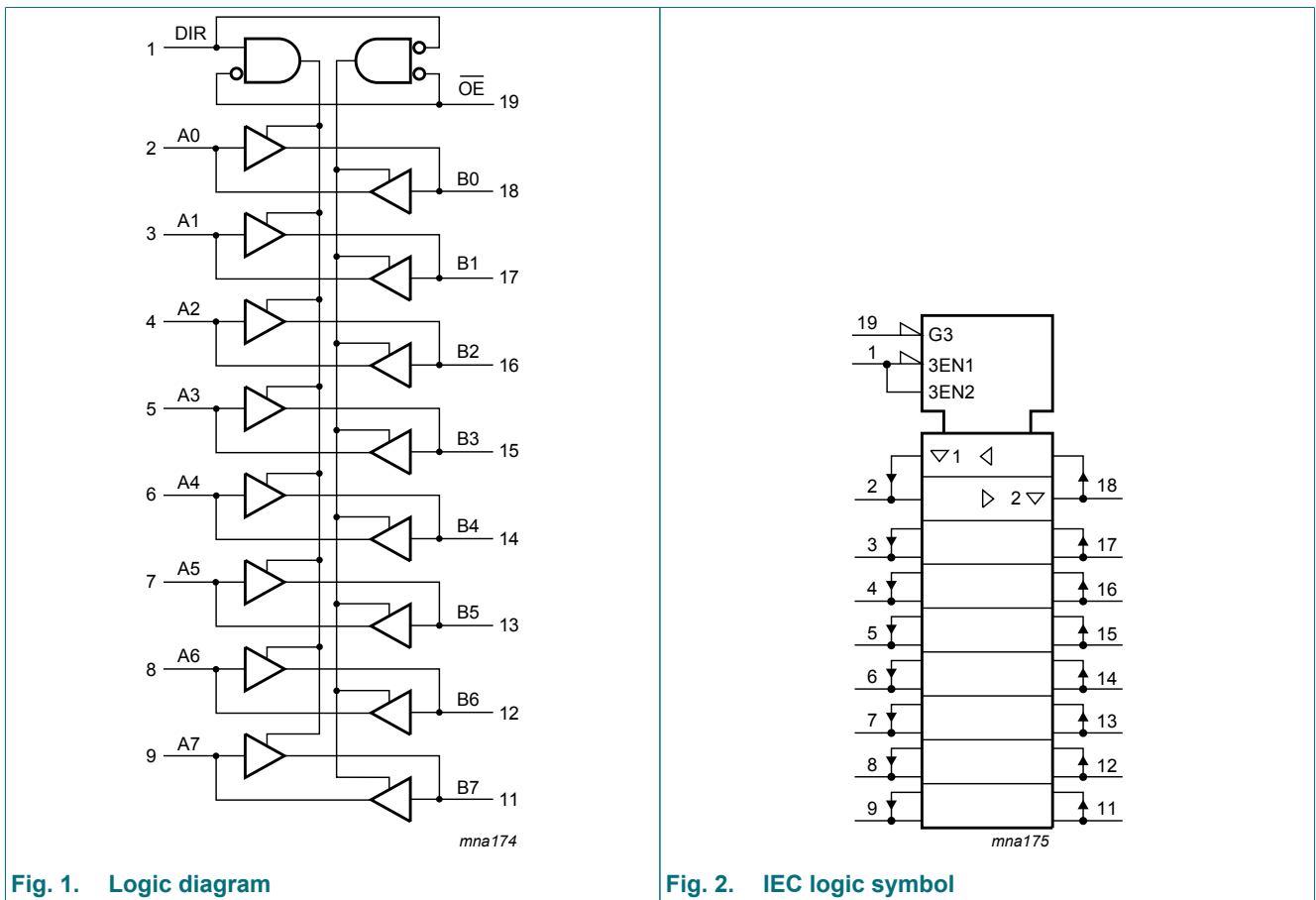
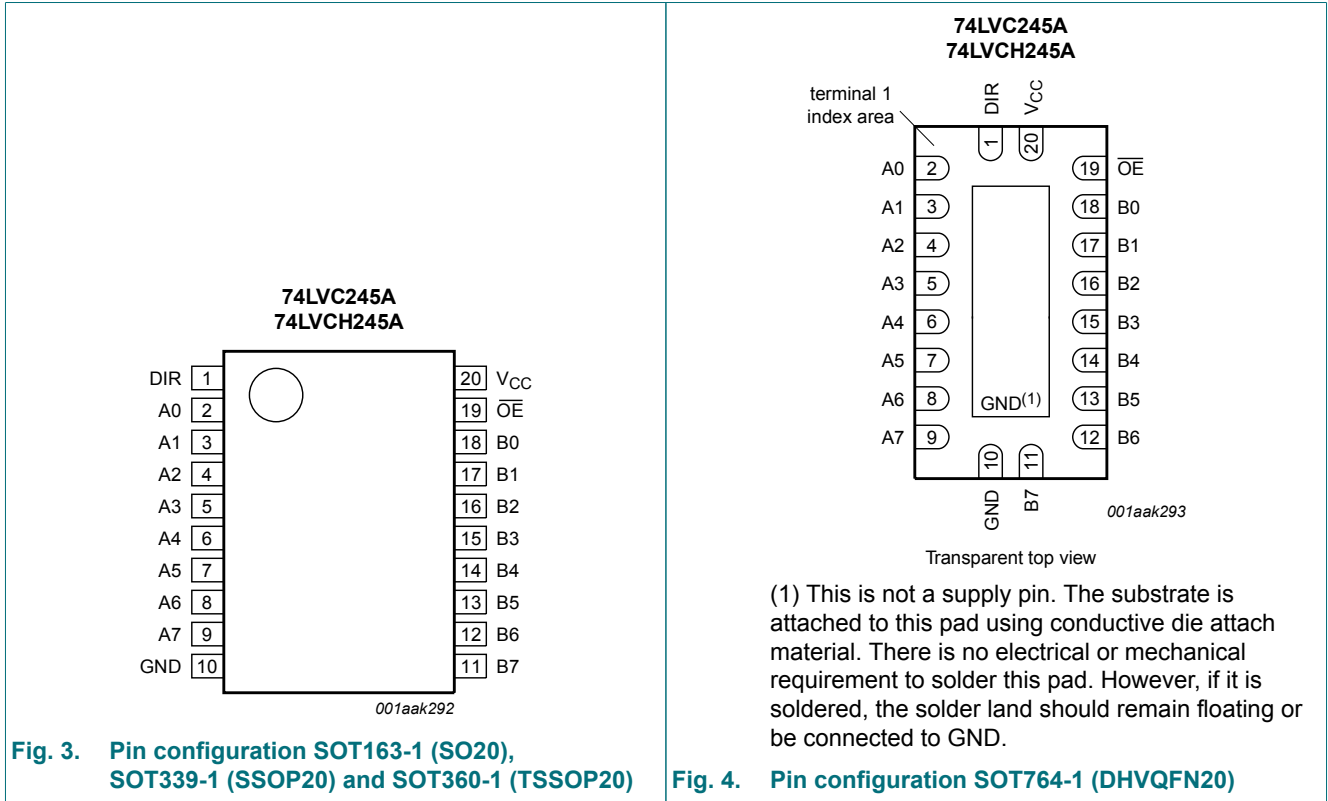


Fig. 1. Logic diagram

Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
OE	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.

Inputs		Inputs/outputs	
OE	DIR	An	Bn
L	L	An = Bn	inputs
L	H	inputs	Bn = An
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW	[2] -0.5	V _{CC} + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.

For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW	0	-	V _{CC}	V
		output 3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit	
			Min	Typ [1]	Max	Min	Max		
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V	
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V	
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V	
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V	
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V	
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V	
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V	
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V	
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V	
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V	
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V	
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}							
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V	
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V	
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V	
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V	
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 3.6 V	[2]	-	±0.1	±5	-	±20	μA
		V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; V _{CC} = 3.6 V	[3]	-	±0.1	±5	-	±20	μA
		V _I or V _O = 5.5 V; V _{CC} = 0.0 V		-	±0.1	±10	-	±20	μA
		V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 3.6 V		-	0.1	10	-	40	μA
		per input pin; V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 2.7 V to 3.6 V		-	5	500	-	5000	μA
		V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}		-	4.0	-	-	-	pF
C _{I/O}	input/output capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}		-	10	-	-	pF	

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I _{BHL}	bus hold LOW current	V _{CC} = 1.65; V _I = 0.58 V [4][5]	10	-	-	10	-	μA
		V _{CC} = 2.3; V _I = 0.7 V	30	-	-	25	-	μA
		V _{CC} = 3.0; V _I = 0.8 V	75	-	-	60	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65; V _I = 1.07 V [4][5]	-10	-	-	-10	-	μA
		V _{CC} = 2.3; V _I = 1.7 V	-30	-	-	-25	-	μA
		V _{CC} = 3.0; V _I = 2.0 V	-75	-	-	-60	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V [4][6]	200	-	-	200	-	μA
		V _{CC} = 2.7 V	300	-	-	300	-	μA
		V _{CC} = 3.6 V	500	-	-	500	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V [4][6]	-200	-	-	-200	-	μA
		V _{CC} = 2.7 V	-300	-	-	-300	-	μA
		V _{CC} = 3.6 V	-500	-	-	-500	-	μA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.

[3] For I/O ports the parameter I_{OZ} includes the input leakage current.

[4] Valid for data inputs of bus hold parts only (74LVCH245A). Note that control inputs do not have a bus hold circuit.

[5] The specified sustaining current at the data input holds the input below the specified V_I level.

[6] The specified overdrive current at the data input forces the data input to the opposite input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nBn; nBn to nAn; see Fig. 5 [2]						
		V _{CC} = 1.2 V	-	17.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.5	14.6	1.5	16.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.4	7.6	1.0	8.7	ns
		V _{CC} = 2.7 V	1.5	3.4	7.3	1.5	9.5	ns
t _{en}	enable time	n $\overline{O}E$ to nAn, nBn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	22.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	8.3	19.5	1.9	22.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.6	10.7	1.5	12.4	ns
		V _{CC} = 2.7 V	1.5	4.8	9.5	1.5	12.0	ns
t _{dis}	disable time	n $\overline{O}E$ to nAn, nBn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	12.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.9	5.5	12.3	2.9	14.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.1	7.1	1.0	8.2	ns
		V _{CC} = 2.7 V	1.5	3.9	8.0	1.5	10.0	ns
t _{sk(o)}	output skew time	[3]	-	-	1.0	-	1.5	ns
		V _{CC} = 1.65 V to 1.95 V	-	7.7	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	11.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	14.4	-	-	-	pF
		C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} [4]				

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

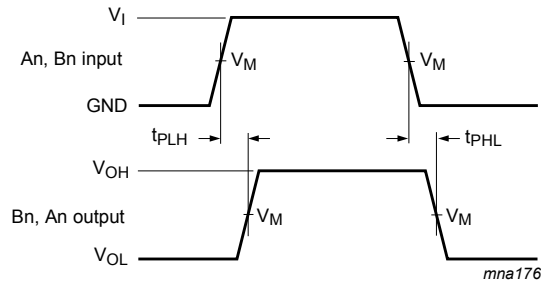
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

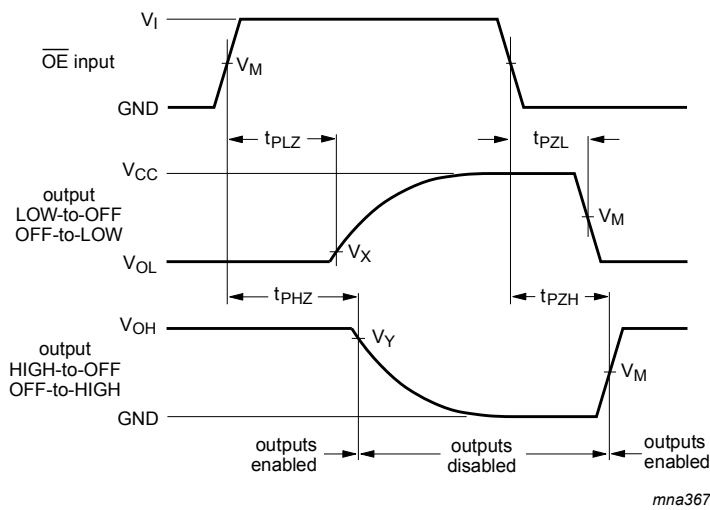
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



See Table 8 for measurement points.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Input (An, Bn) to output (Bn, An) propagation delays and output transition times

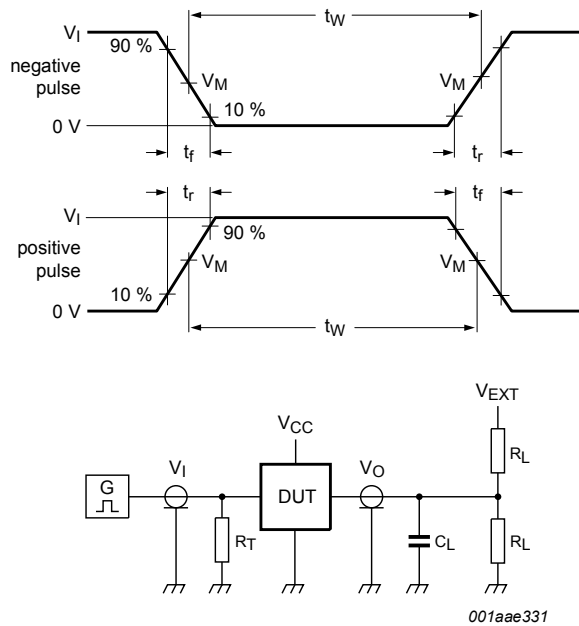


See Table 8 for measurement points.
 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Enable and disable times

Table 8. Measurement points

Supply voltage	V_M	Input		
V_{CC}		V_I	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	2.7 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	2.7 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

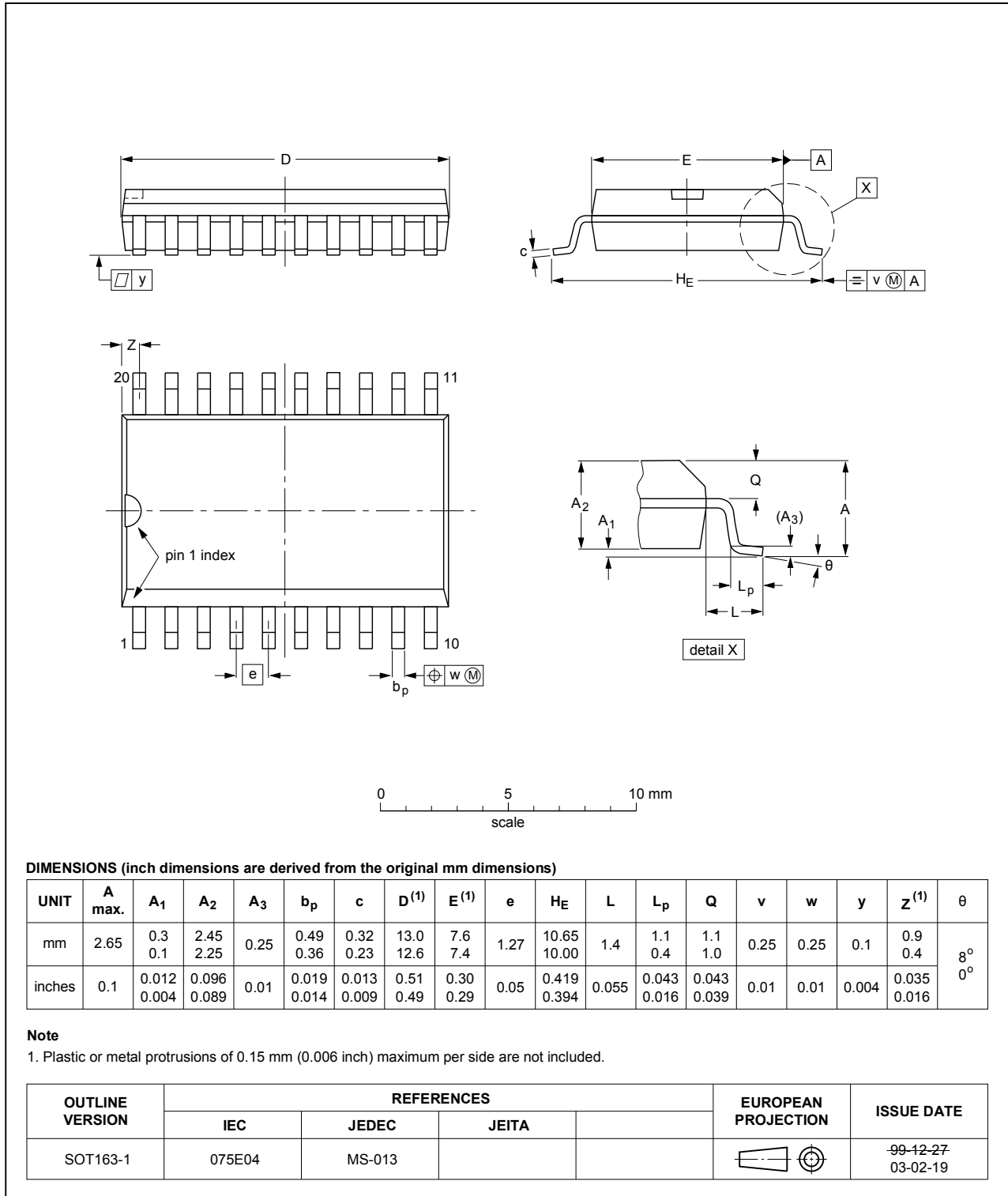


Fig. 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

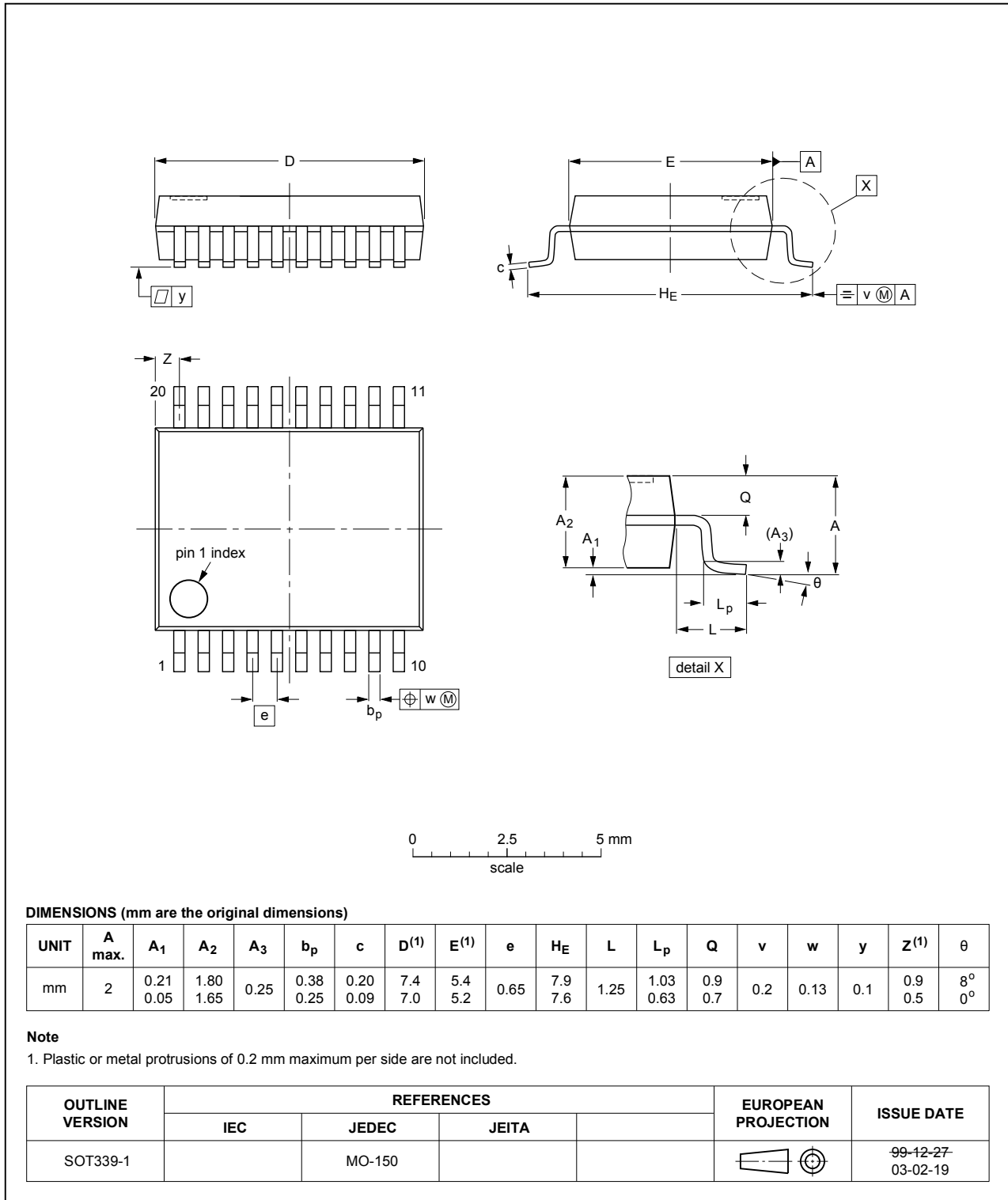


Fig. 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

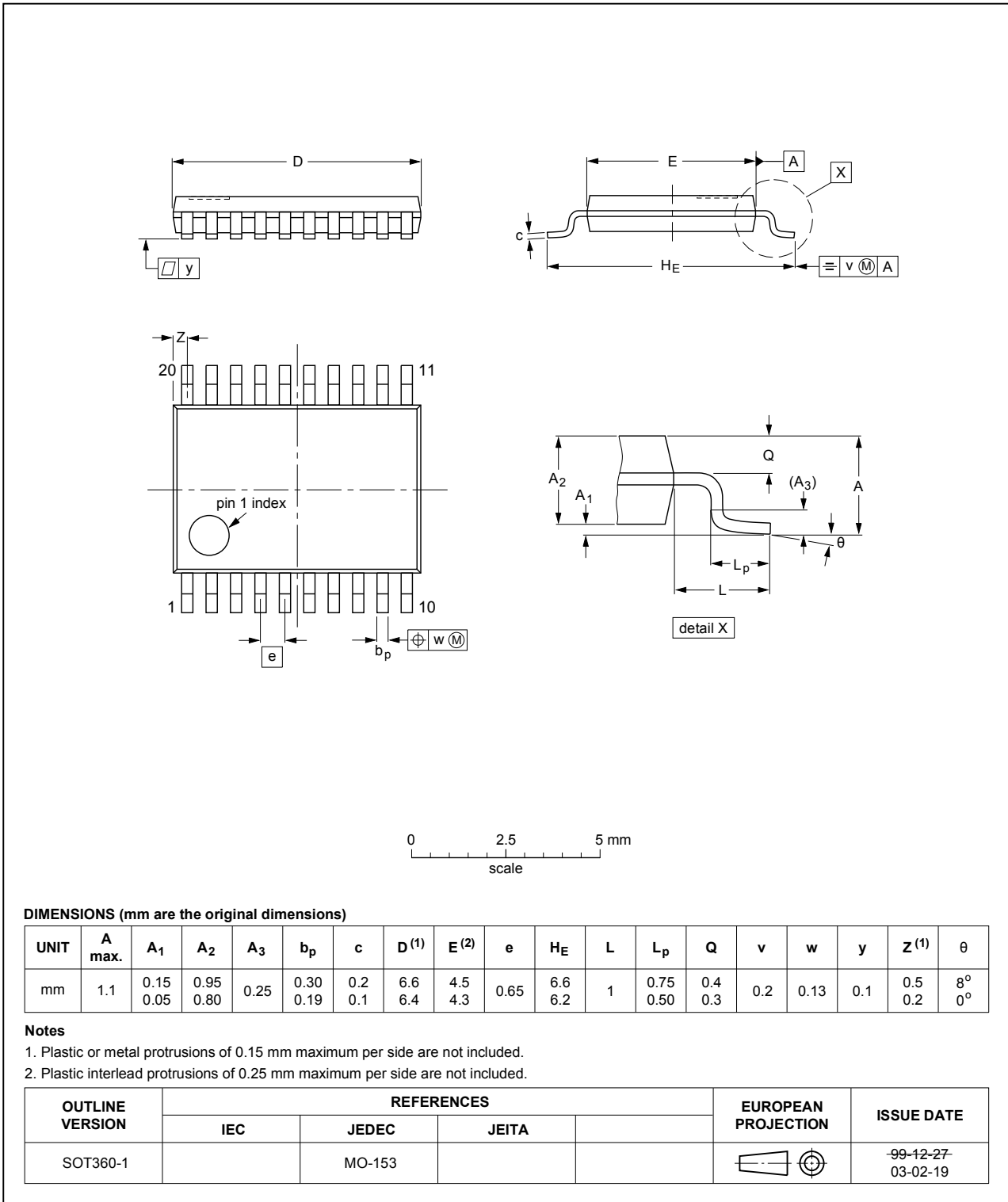


Fig. 10. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

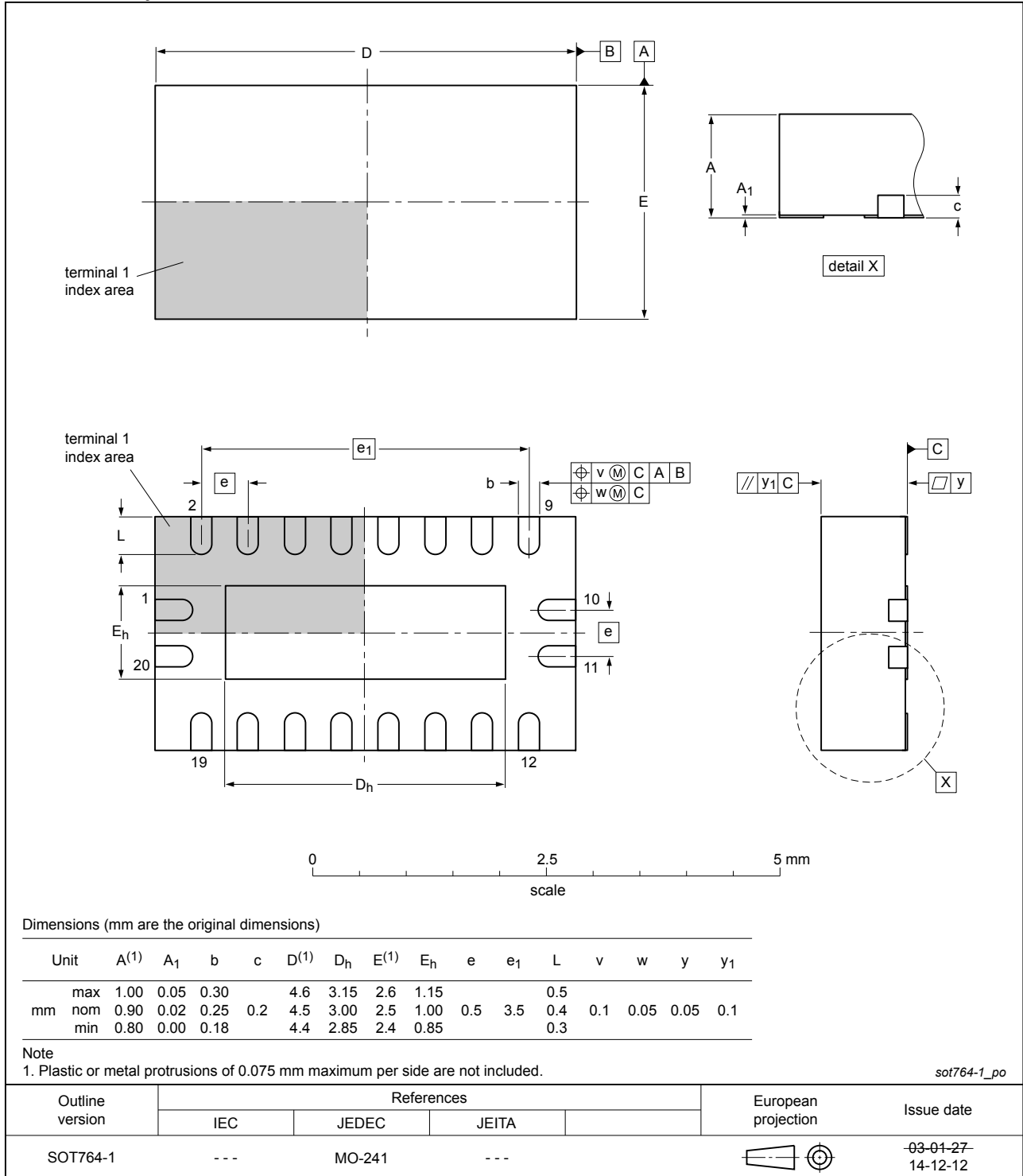


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH245A v.9	20180911	Product data sheet	-	74LVC_LVCH245A v.8
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74LVC245ABX and 74LVCH245ABX (SOT1045-2) removed. Package outline drawing of SOT764-1 updated. 			
74LVC_LVCH245A v.8	20130628	Product data sheet	-	74LVC_LVCH245A v.7
Modifications:	<ul style="list-style-type: none"> For type numbers 74LVC245ABX and 74LVCH245ABX DHXQFN20U (SOT1045-1) has changed to DHXQFN20 (SOT1045-2). 			
74LVC_LVCH245A v.7	20120405	Product data sheet	-	74LVC_LVCH245A v.6
Modifications:	<ul style="list-style-type: none"> Table note 4 of Table 6: corrected (errata) 			
74LVC_LVCH245A v.6	20111125	Product data sheet	-	74LVC_LVCH245A v.5
Modifications:	<ul style="list-style-type: none"> Table 4, Table 5, Table 6, Table 7, and Table 9: values added for lower voltage ranges. 			
74LVC_LVCH245A v.5	20090825	Product data sheet	-	74LVC_LVCH245A v.4
74LVC_LVCH245A v.4	20090703	Product data sheet	-	74LVC_LVCH245A v.3
74LVC_LVCH245A v.3	20030507	Product specification	-	74LVC245A_74LVCH245A v.2
74LVC245A_74LVCH245A v.2	20020620	Product specification	-	74LVC245A_74LVCH245A v.1
74LVC245A_74LVCH245A v.1	19971219	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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